

# POWER CRUNSH X1P INTEL SKL-H SYSTEM DIAGRAM

01

<b>+3V/+5V S5</b>
PG.40
<b>+1.0V/+1.35VSUS</b>
PG.42,41
<b>CPU Core</b>
PG.44~46
<b>DDR3L</b>
PG.41
<b>Charge</b>
PG.39

**SODIMM1**  
Max. 8GB  
STD PG.17

**SODIMM2**  
Max. 8GB  
STD PG.18

**INTEL SkyLake-H**  
Processor : Daul / Quad Core  
Power : 45 (Watt)  
Package : BGA1400  
Size : 42 x 28 (mm)

**NVIDIA N16P-GT**  
Package 29\*29mm  
**40W**  
PAGE 19~23

VRAM DDR3 x 8  
256M X 16 X 8  
900Mhz  
PAGE 24~27

**Stackup**

TOP  
GND  
IN1  
IN2  
VCC  
IN3  
GND  
BOT

**mSATA/NGFF**  
PG.35

**HDD**  
PG.37

**ODD**  
PG.37

**INTEL PCH Lynx Point**  
Power : Watt  
Package : FCBGA837  
Size : 23 x 23 (mm)  
PG.9~15

**USB3.0 Ports**  
combo x2+x1  
PG.32; PG.35

**Webcam**  
PG.16

**Touch Screen**  
Elan EKTH3915 for 14", 15"  
Elan EKTH3918 for 17"  
PG.33

PG.34  
**PCI-E x 1**  
LANE2  
**LAN (DB)**  
RTL8111GSH  
10/100/1000 PG.32  
LANE1  
**WLAN BT COMBO**  
PG.37  
USB 2.0  
PORT10

**PCI-E x 1**  
LANE3  
**Accelerometer**  
PG.35  
SMBUS  
**Card Reader**  
RTS5237 (DB)  
PG.32  
LPC

**KBC**  
ITE IT8987E/BX  
PG.38  
LPC Interface  
TPM  
SLB9656TT1.2  
PAGE 35  
KB  
PG.34  
TP  
PG.34  
ROM  
PG.12  
FAN  
PG.34

**SLG3NB3454**  
GreenCLK (Ni)  
PAGE 35  
25MHz

**AUDIO CODEC**  
ALC 3241  
PG.30

**Headphone amplifier**  
TPA6133A2  
PAGE 32  
Hp MIC

**Combo Jack**  
PAGE 30

**Subwoofer amplifier**  
ALC1301 (Reserve)  
PAGE 33

**Speaker**  
PAGE 30

**Dual Digital MIC**  
PAGE 30

**USB3.0 Ports**  
3D Camera  
PG.31

USB3.0 Re-Driver IC  
PS8713B1QFN24GTR2  
PG.31  
R

20150616\_1200

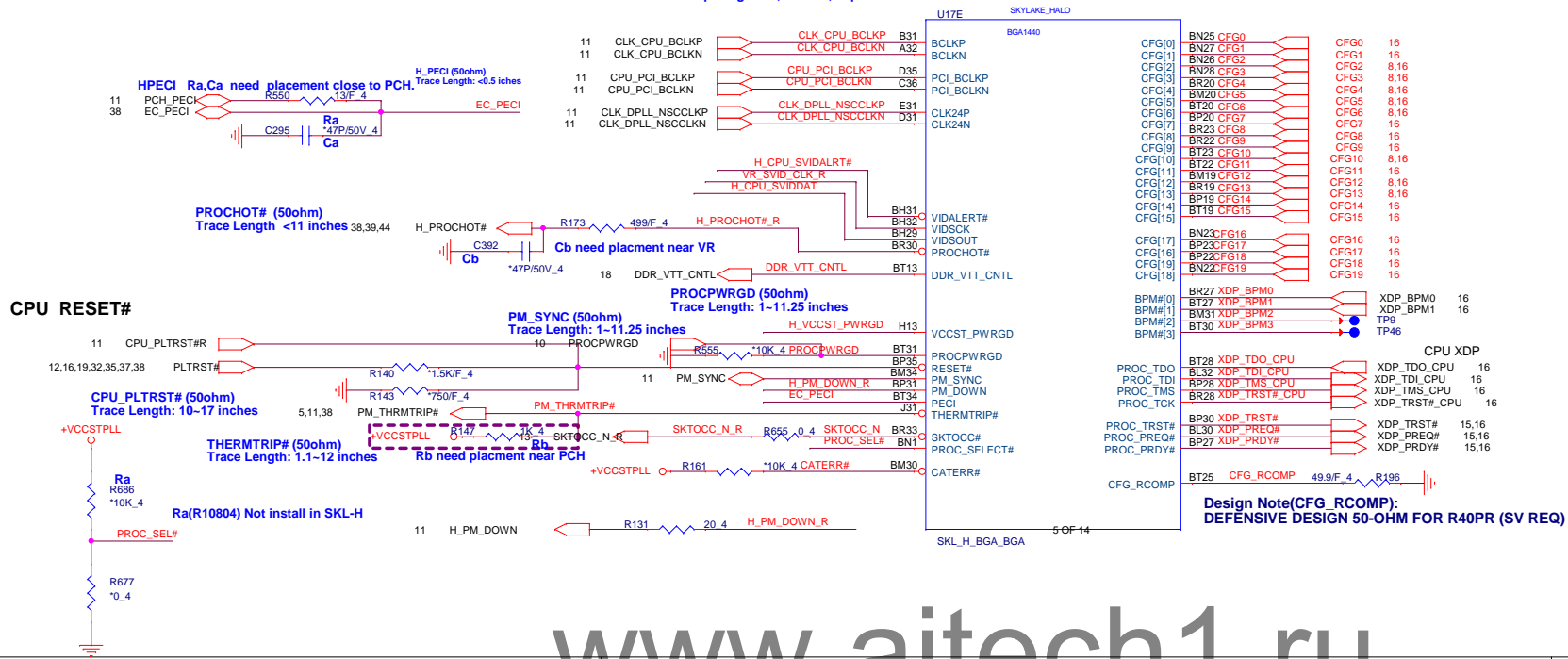


**PROJECT : Y19C**  
Quanta Computer Inc.

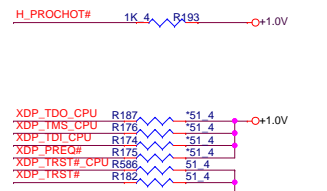
Size Custom Document Number **BLOCK DIAGRAM** Rev 2A  
Date: Tuesday, June 16, 2015 Sheet 1 of 51

# SKYLAKE Processor (CLK,MISC,JTAG)

Host CLK:  
Trace length < 11000 MILS  
Trace spacing = 15, 20 MILS, Impedence 90 ohm



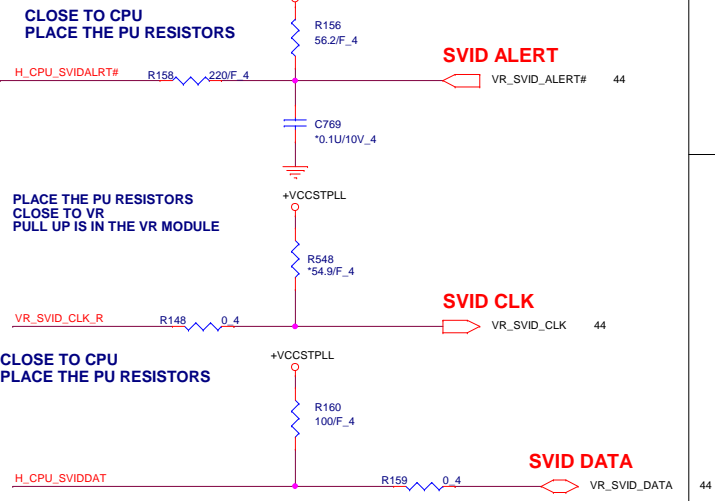
## Processor pull-up (CPU)



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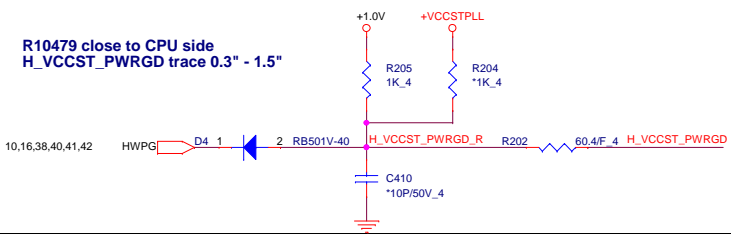
## CPU CORE SVID

Layout note: need routing together and ALERT need between CLK and DATA.

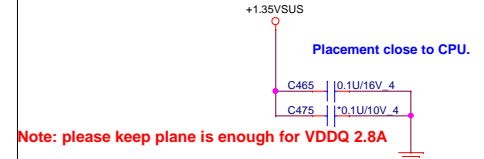


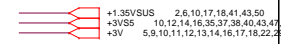
## HVPD

R10479 close to CPU side  
 $H\_VCCST\_PWRGD$  trace 0.3" - 1.5"

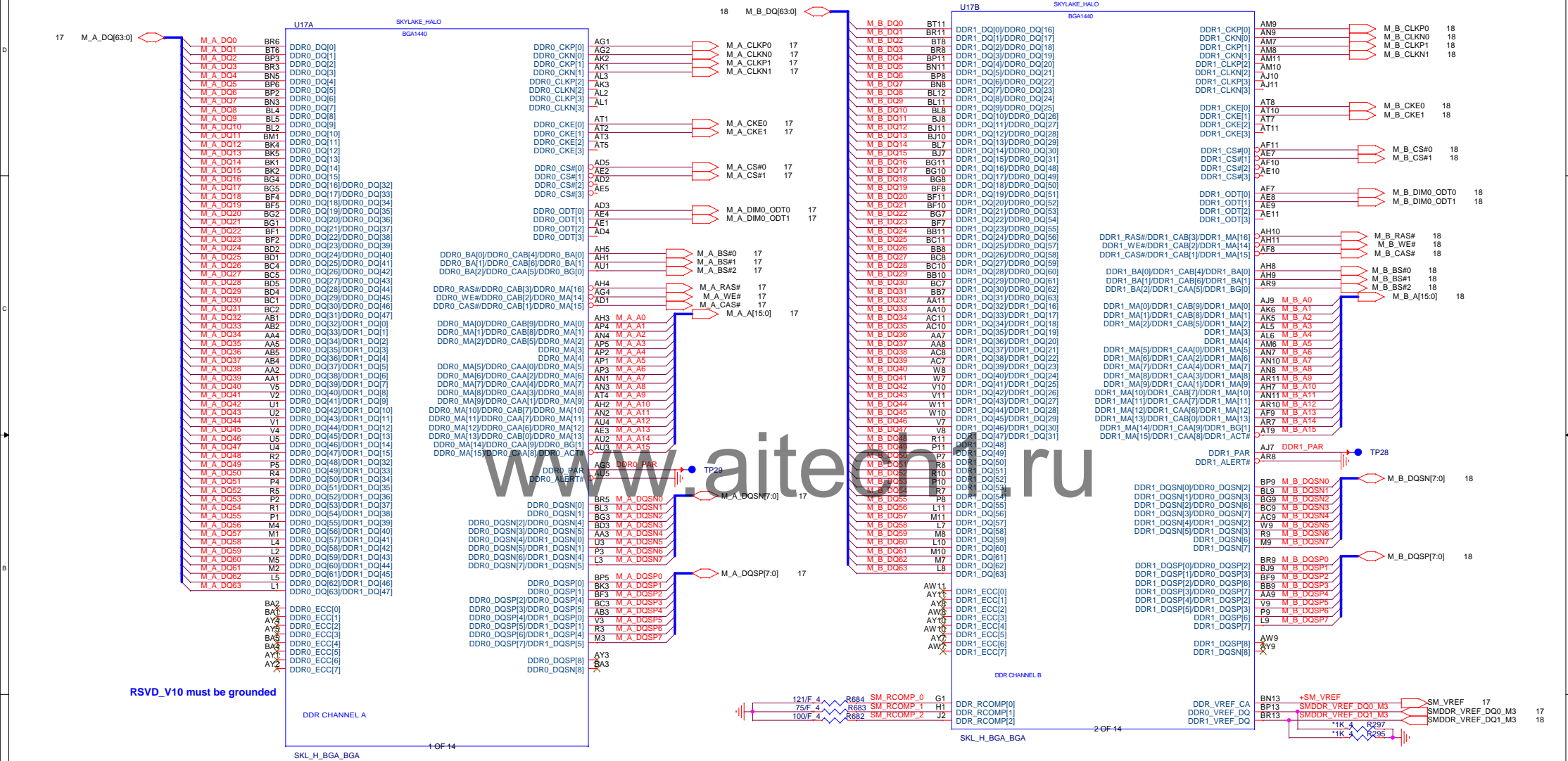


## CPU VDDQ






## SKYLAKE Processor (DDR3)

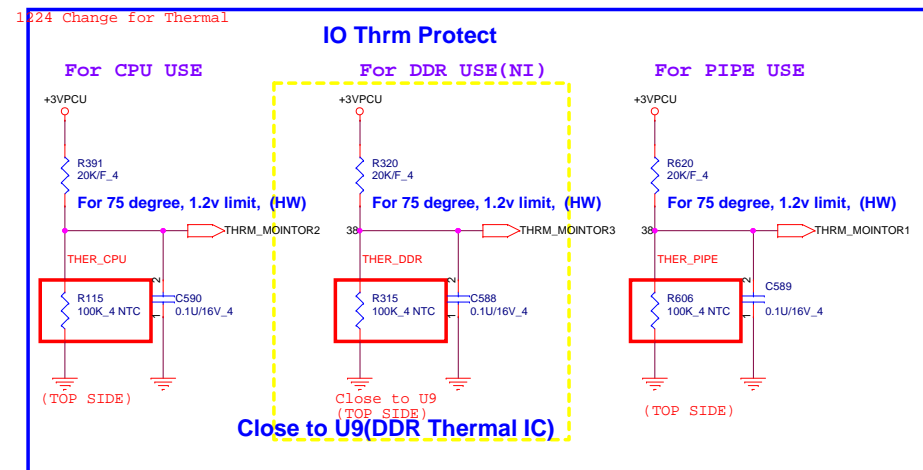
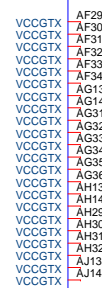




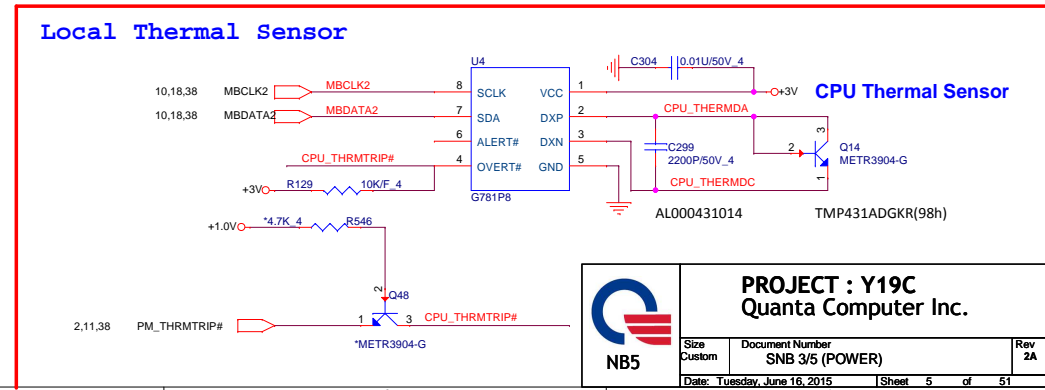
Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A

### Thrm Protect SCH

	+VCC_CORE	7,44,45
	+1.35VSUS	2,6,10,17,18,41,43,50

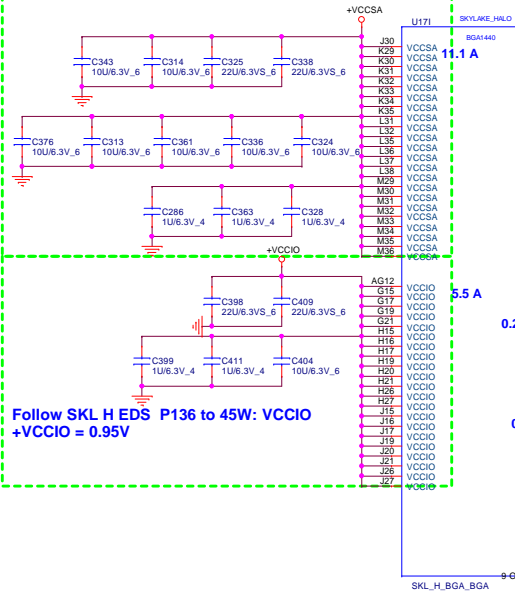


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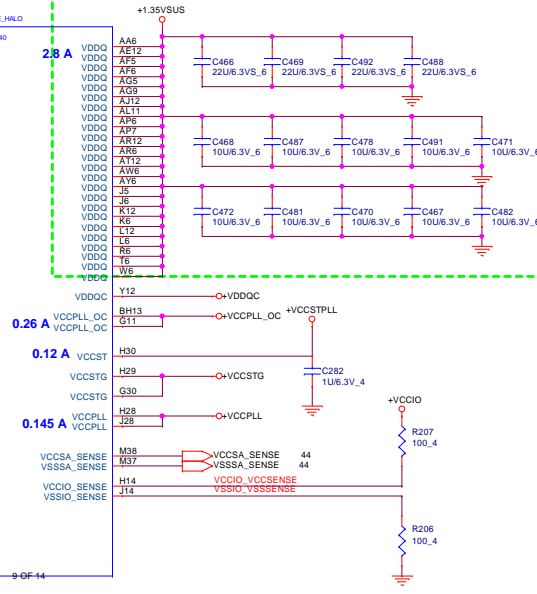


VCC Output Decoupling Recommendations		

Follow SKL H EDS page 135 to 45W(GT2): VCCSA=11.1A (GTx)

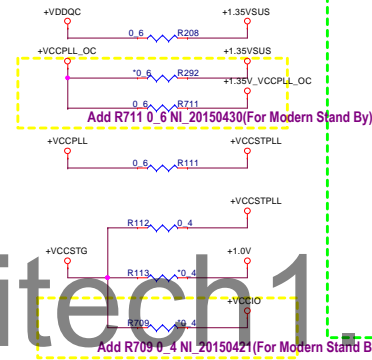


Follow SKL H EDS page 135 45W: VDDQ=2.8A

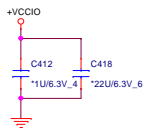
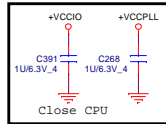
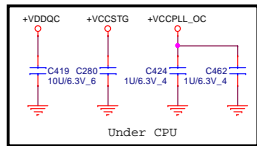
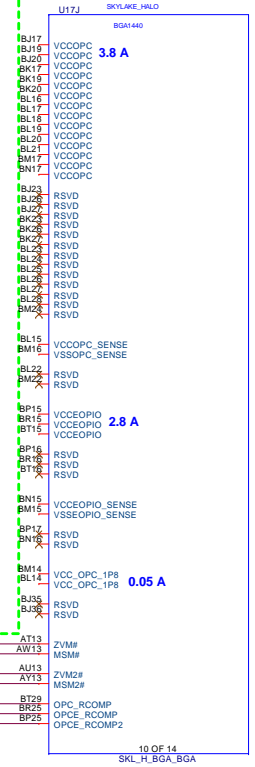


Change R292 from I to NI\_20150522

Change R711 from NI to I\_20150522



EDRAM Only, PLACE CAPS IN ACK SIDE

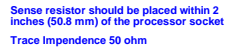


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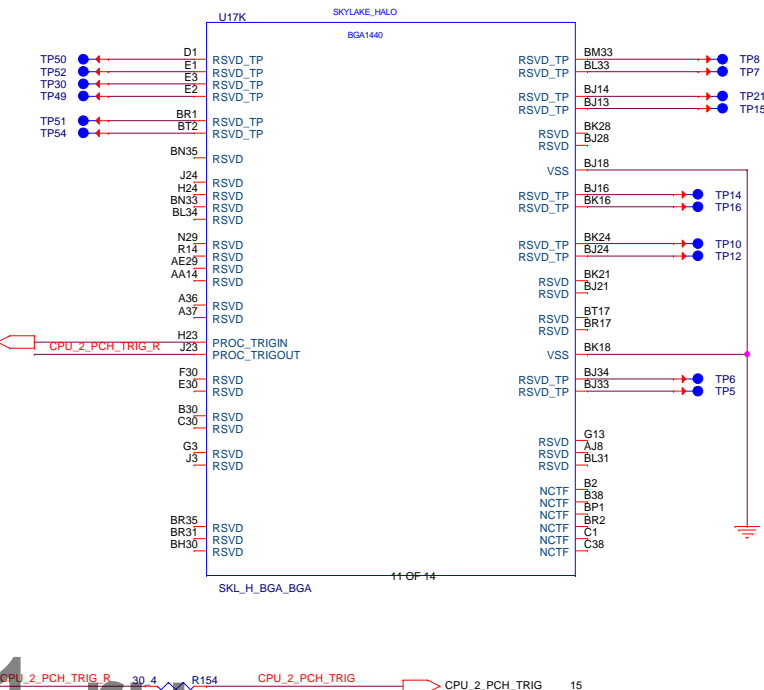
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## SKL-HProcessor (GND)



## SKL-H Processor (RESERVED, CFG)

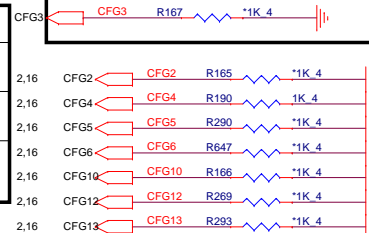


## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

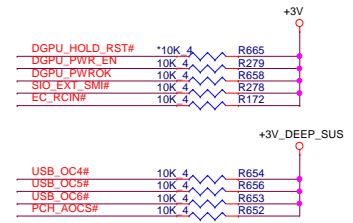
	1	0	2,16

0 Enable; SET DFX ENABLED BIT IN DEBUG  
1 , Disable;

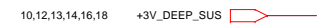


**PROJECT : Y19C**  
**Quanta Computer Inc.**

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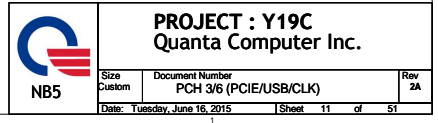
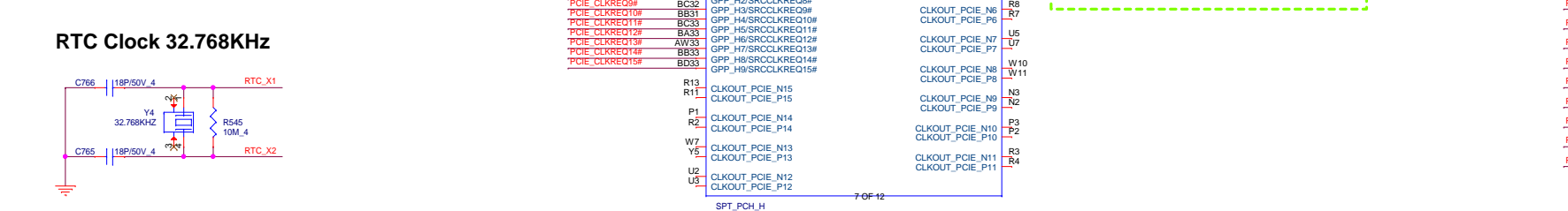


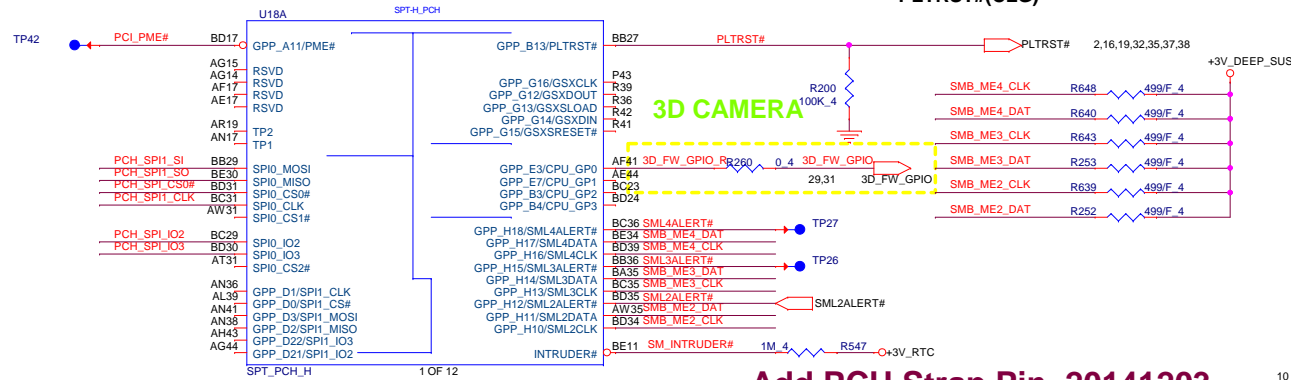
**BOM:DIS only**











## Add PCH Strap Pin\_20141203

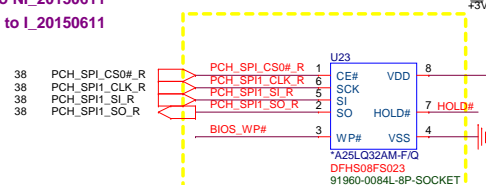
Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP (QE
Winbond	8MB	AKE3EP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)

## PCH SPI ROM(CLG)

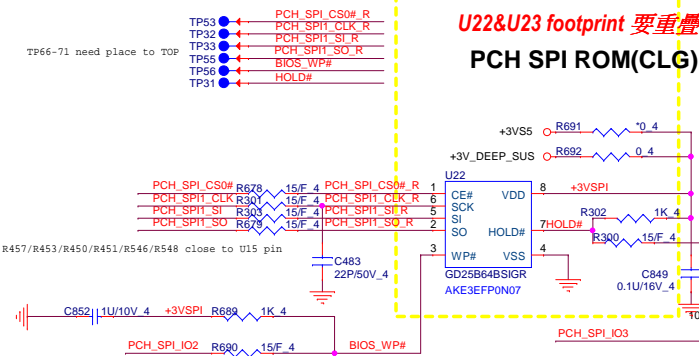
Vender	Size	P/N
EON	8MB	AKE3EZNOQ01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGNOQ01 (GD25B64BSIGR)
Socket		DFHS08FS023

Change U23 from I to NI\_20150611  
Change U22 from NI to I\_20150611

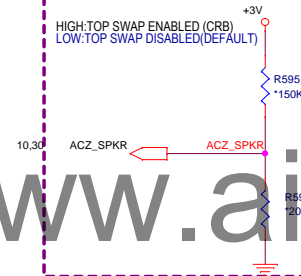
### 4M SPI ROM Socket



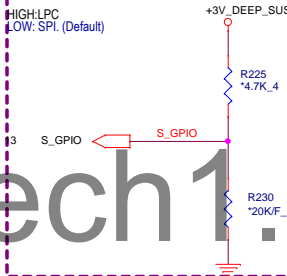
**U22&U23 footprint 要重疊**  
**PCH SPI ROM(CLG)**



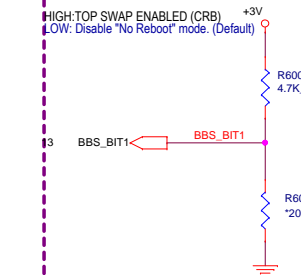
## TOP SWAP OVERRIDE STRAP



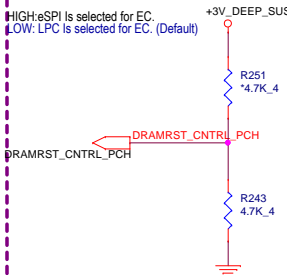
**BOOT SELECT STRAP**



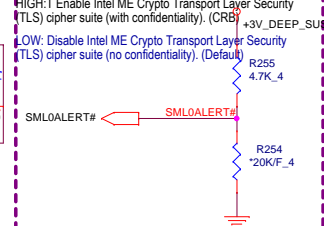
**NO REBOOT IF SAMPLED HIGH**



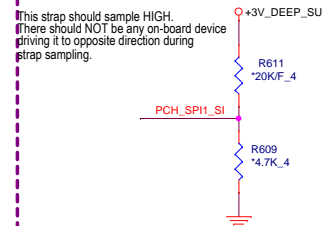
## ESPI/LPC SELECT STRAP



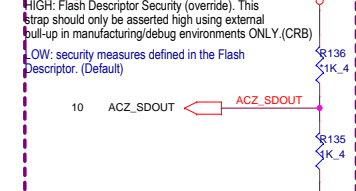
**TLS CONFIDENTIALITY ENABLED**



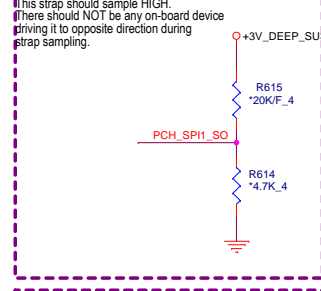
## RESERVED



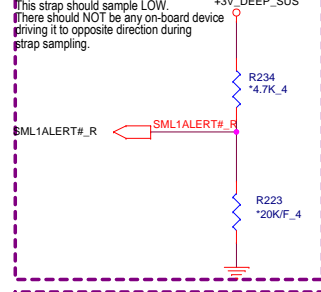
**TLS CONFIDENTIALITY ENABLED**



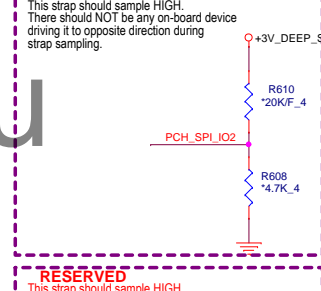
**RESERVED**  
This area should be reserved for future use.



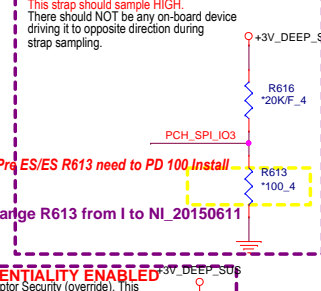
## RESERVED



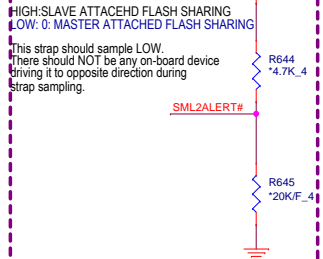
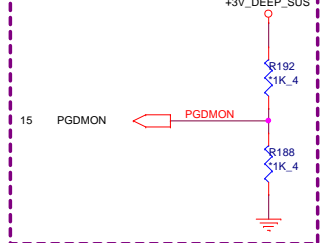
## RESERVE



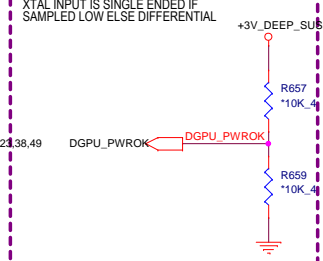
**RESERVE**  
This stop should



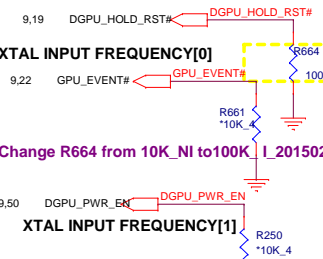
ESPI FLASH SHARING MODE

DFX TEST MODE QUALIFIER FOR OTHER DFX STRAP  
WHEN SAMPLED LOW +3V DEEP SUS

DFX TEST MODE  
XTAL INPUT IS SINGLE E



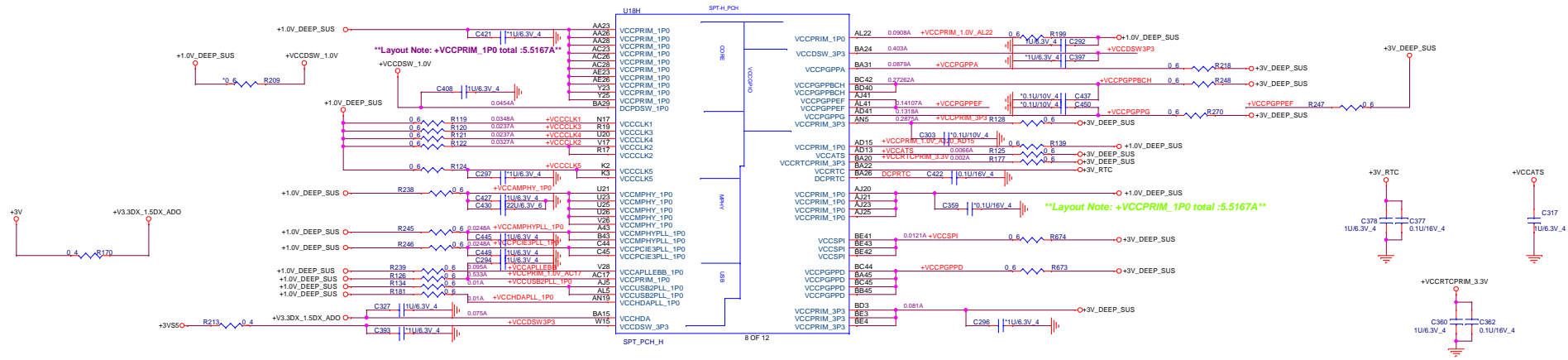
## RING OSCILLATOR BYPASS



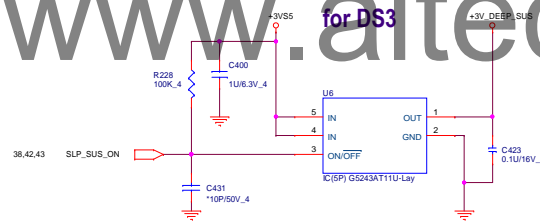
**PROJECT : Y19C**  
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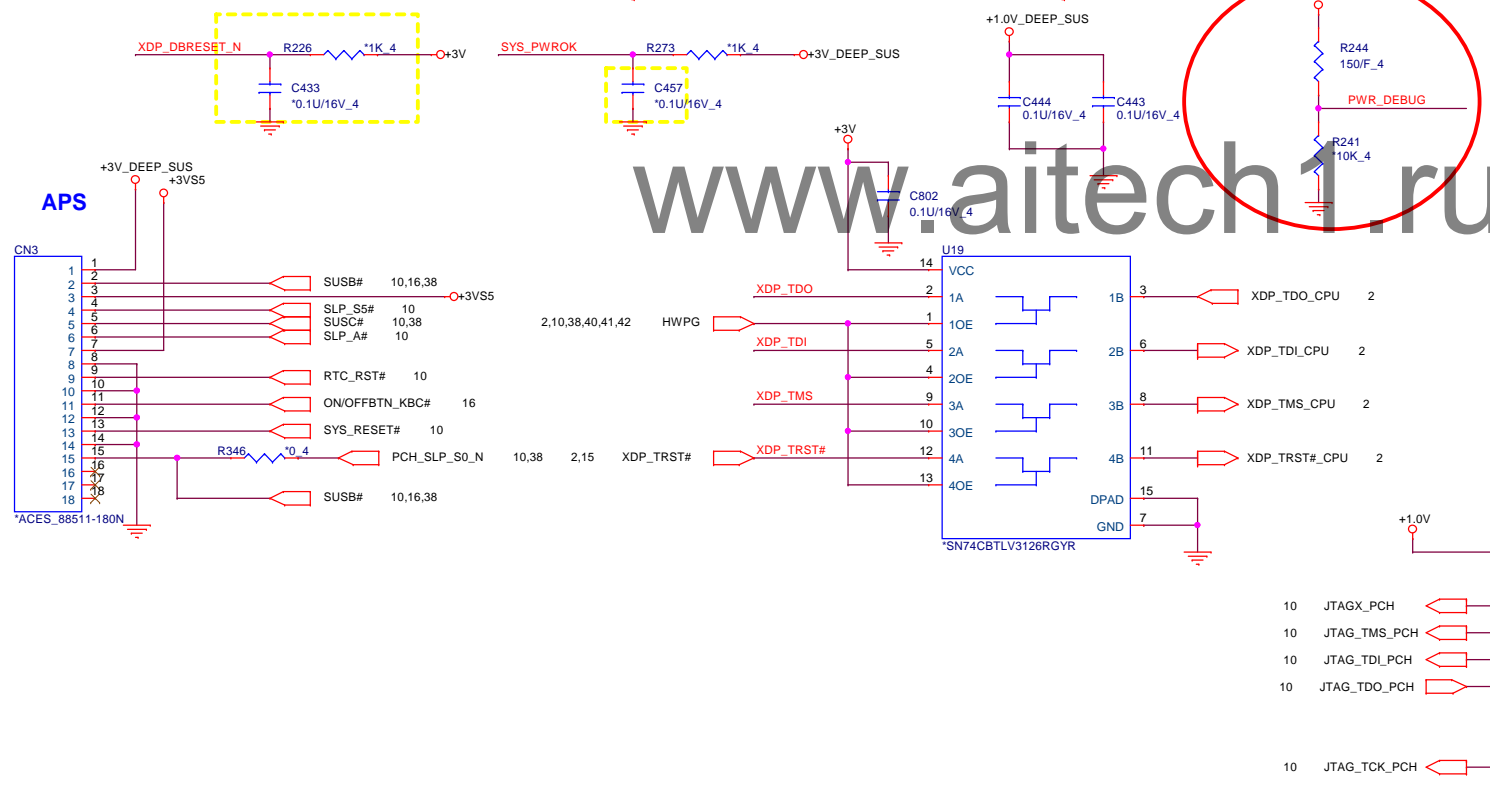
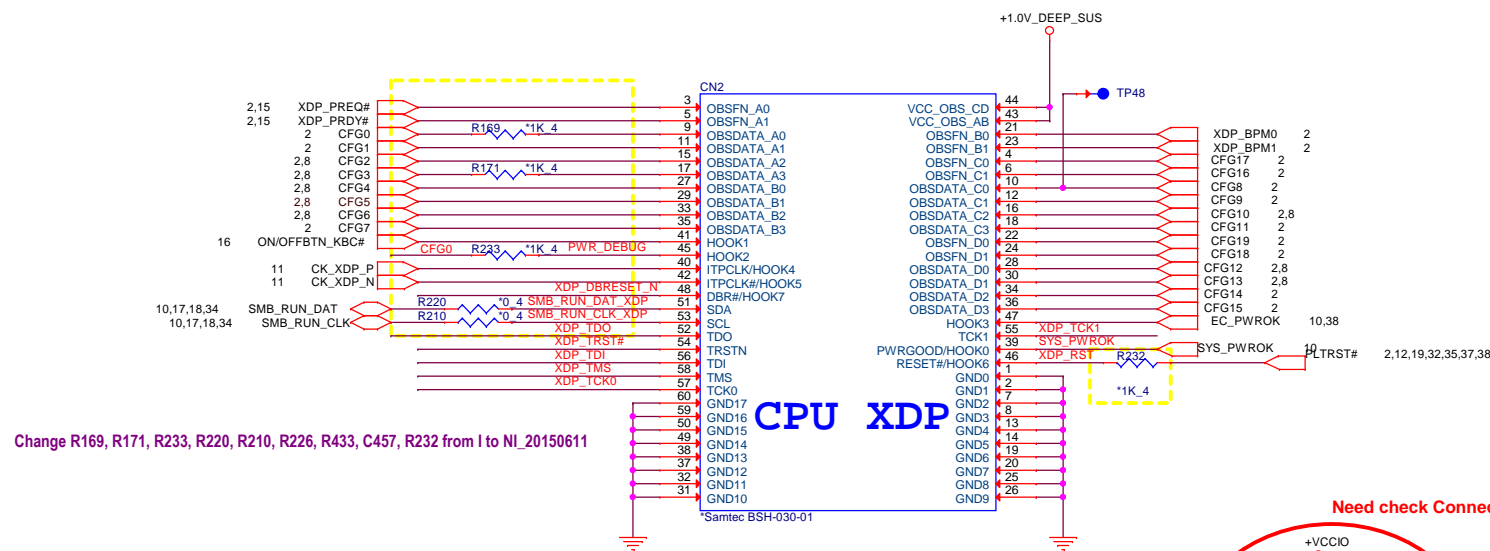


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9.10.12.13.16.18 +3V\_DEEP\_SUS

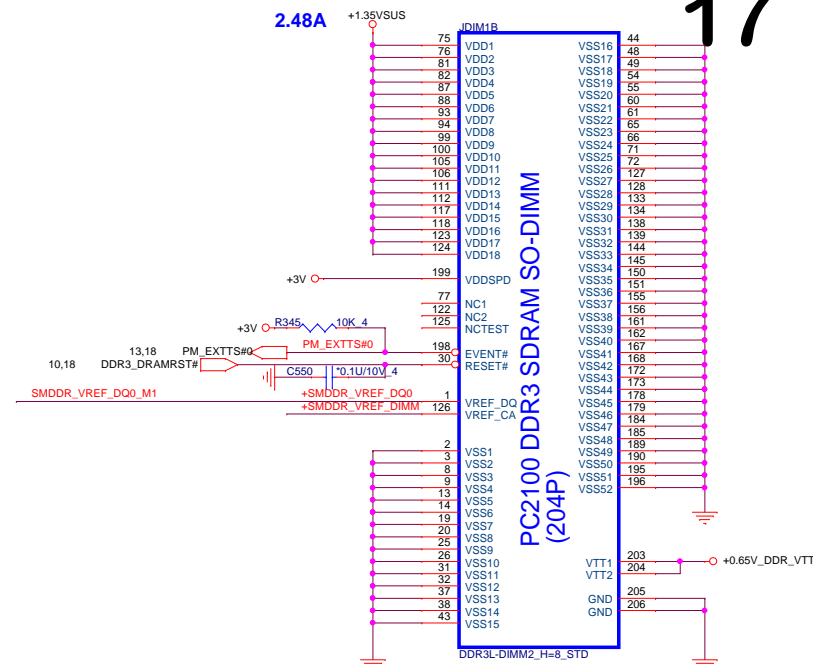
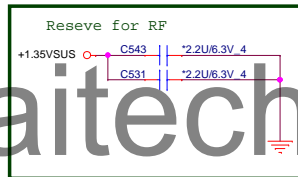
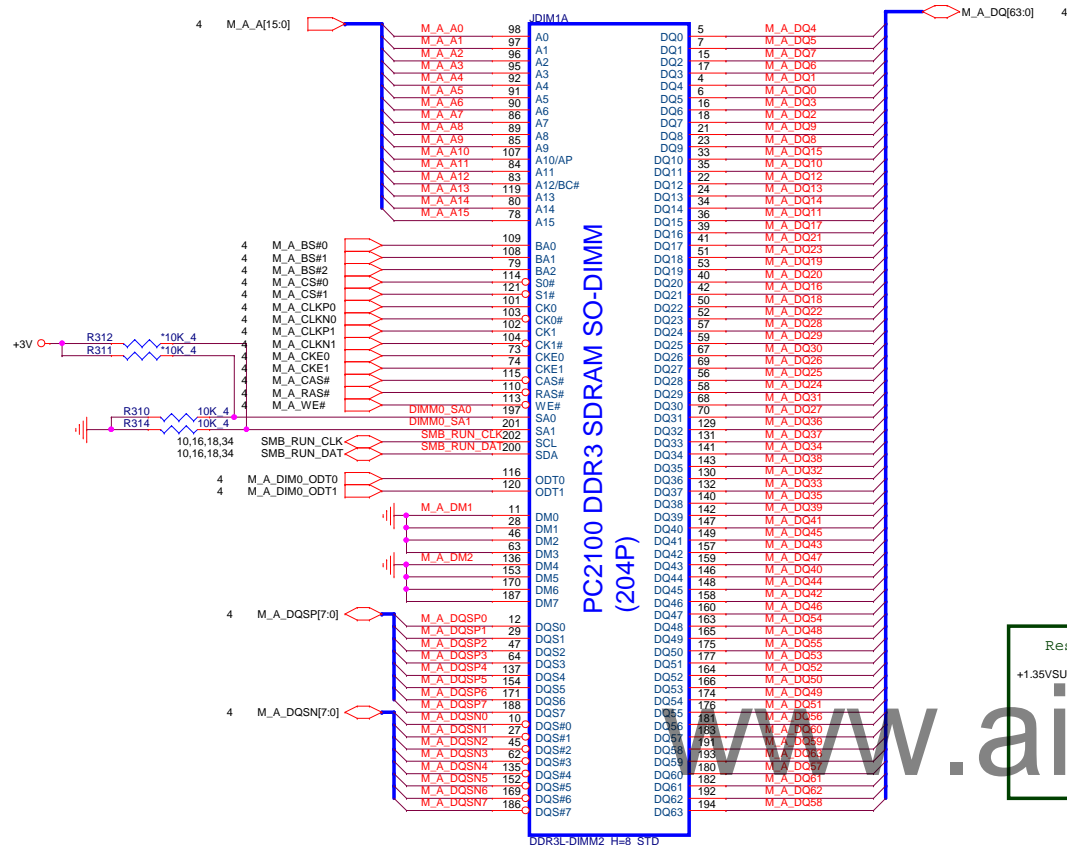




**PROJECT : Bellagio**  
**Quanta Computer Inc.**

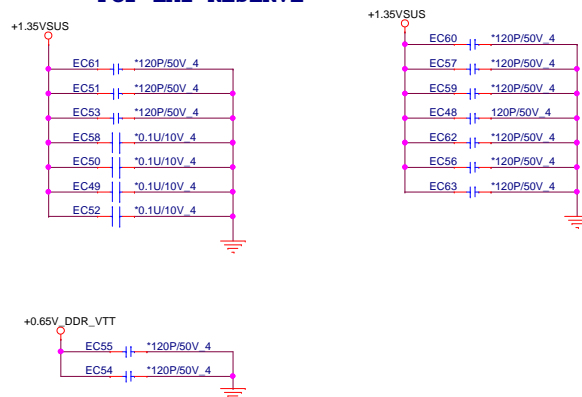
Size	Document Number	Rev
NB5	22 -- HSW XDP & APS	1A
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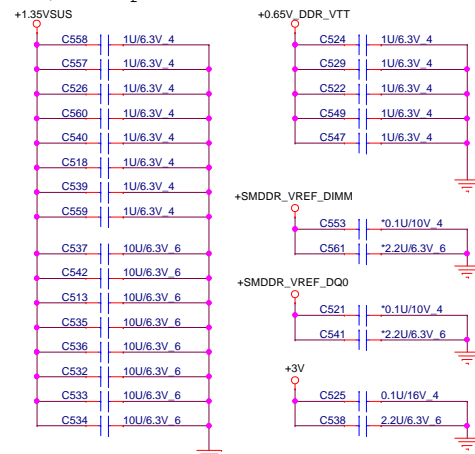


+SMDDR\_VREF\_DIMM 18  
+1.35VSUS 2,6,10,18,41,43,50  
+3V 5,9,10,11,12,13,14,16,18,22,29,30,31,32,34,35,36,37,38,44,47,48

### For EMI RESERVE

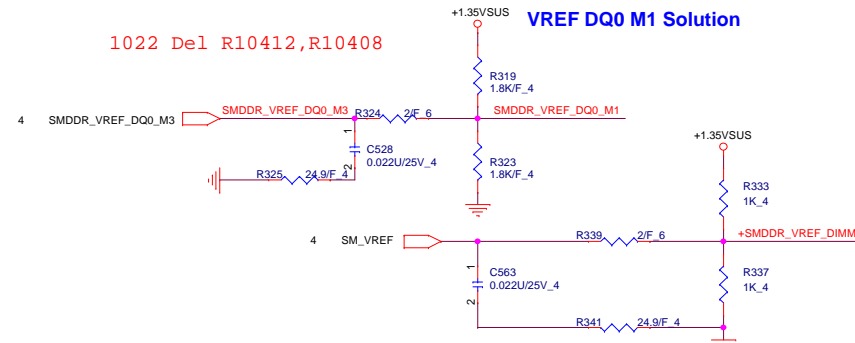


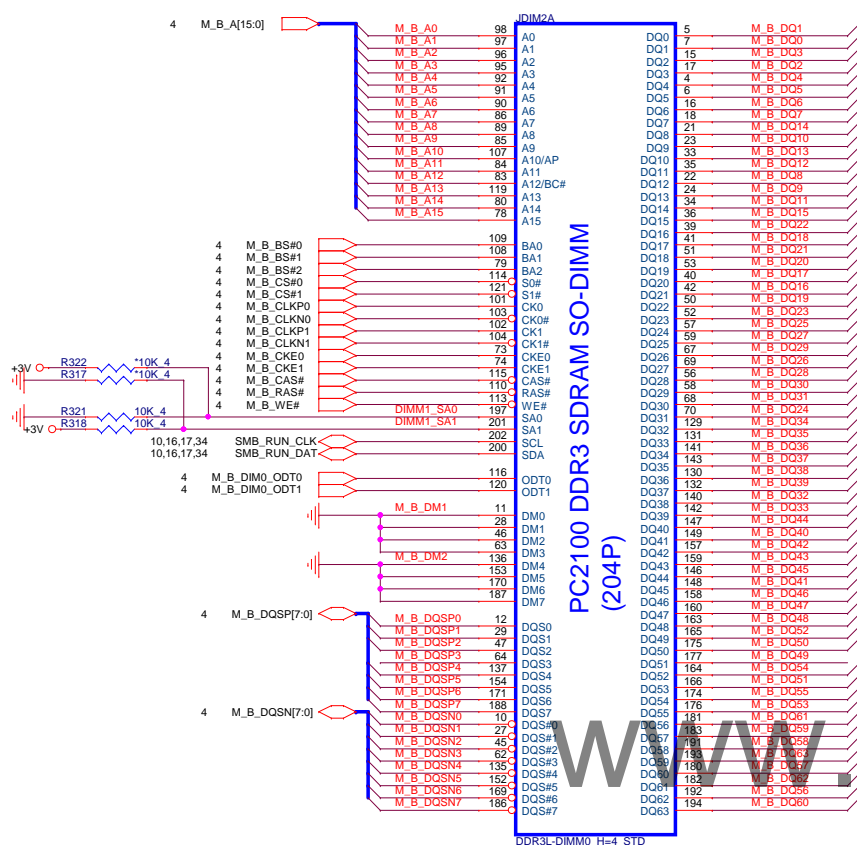
1uF/10uF 4pcs on each side of connector



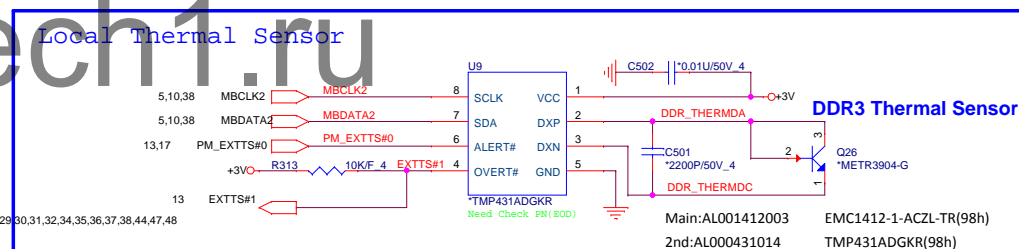
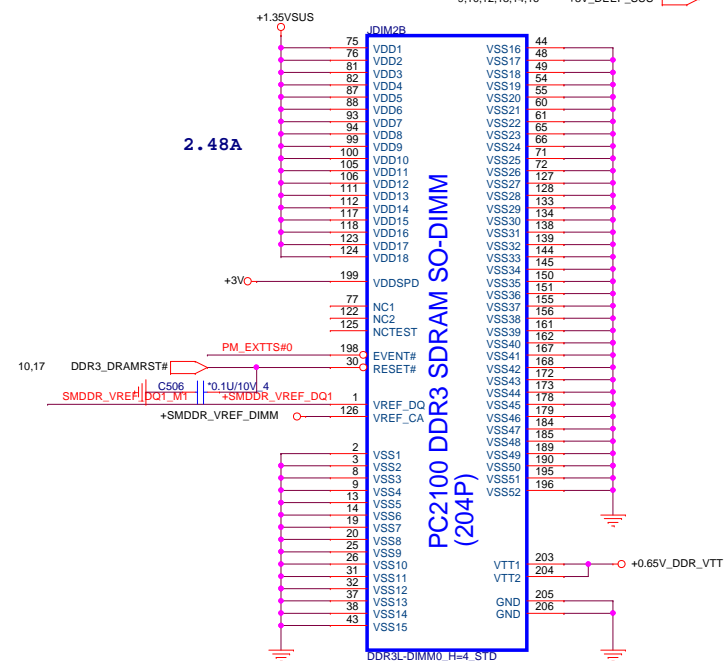
1022 Del R10412, R10408

### VREF DQ0 M1 Solution

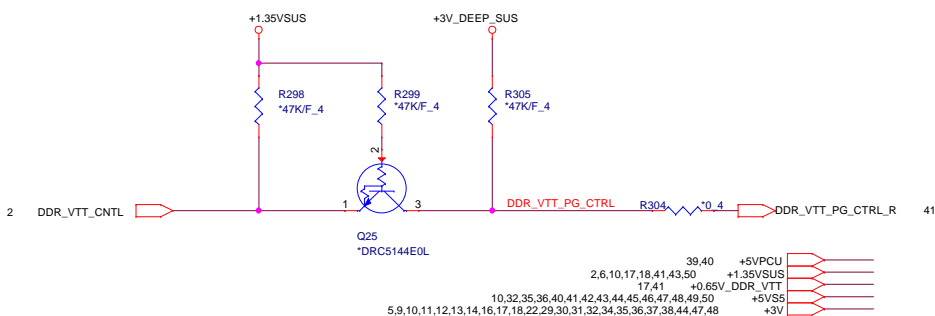




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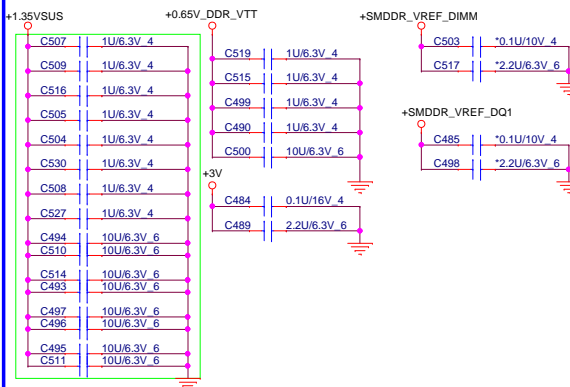


### Co-lay for ODT From Intel MOW, ODT directly connection to CPU

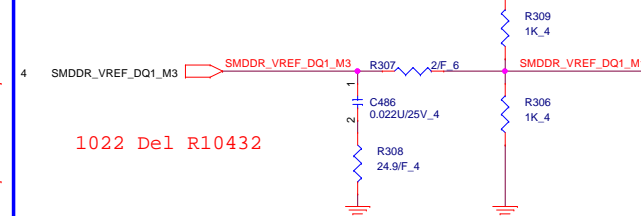


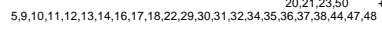
### Place these Caps near So-Dimm1.

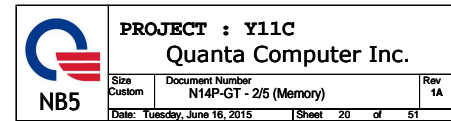
1uF/10uF 4pcs on each side of connector

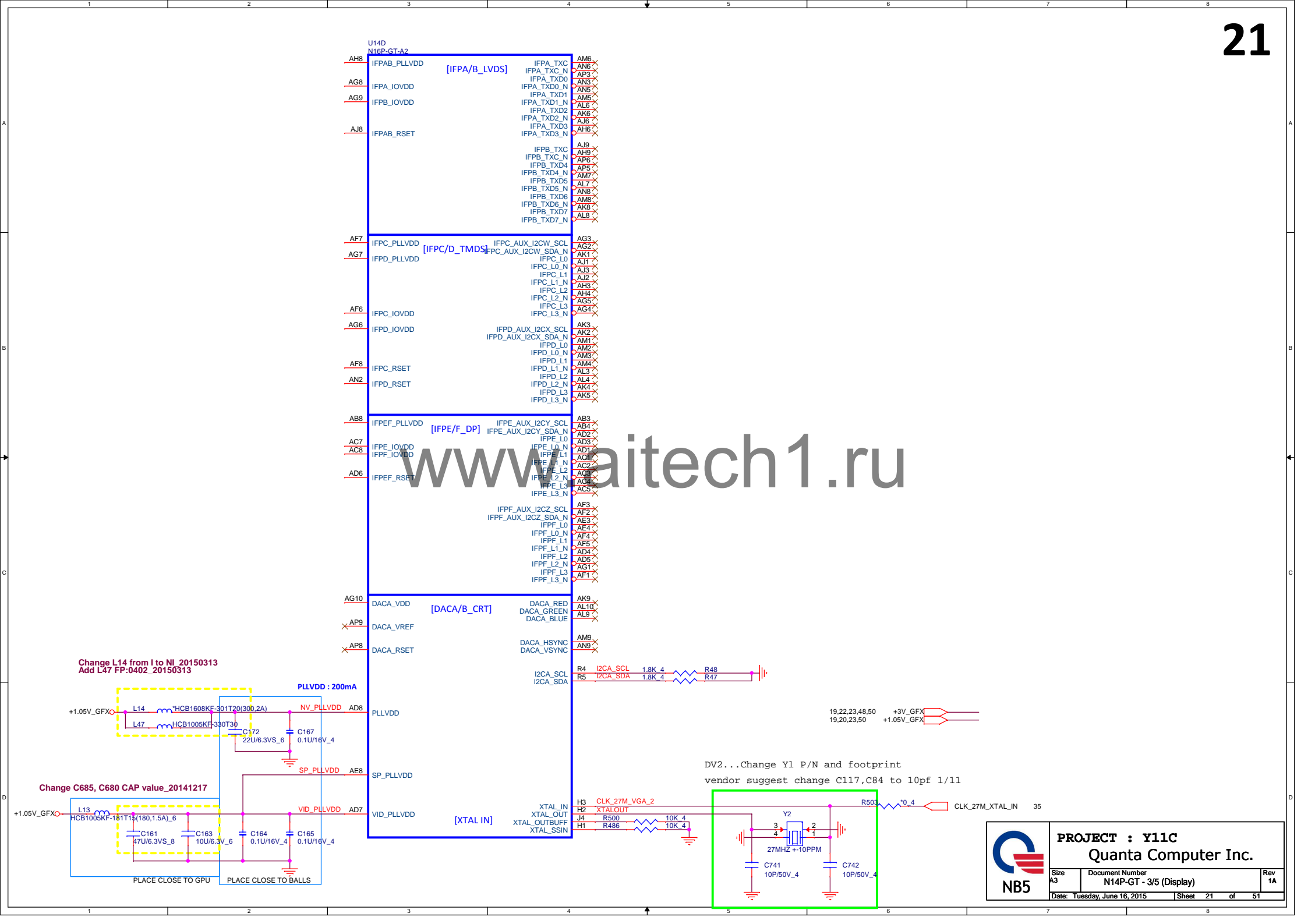


### VREF DQ1 M1 Solution









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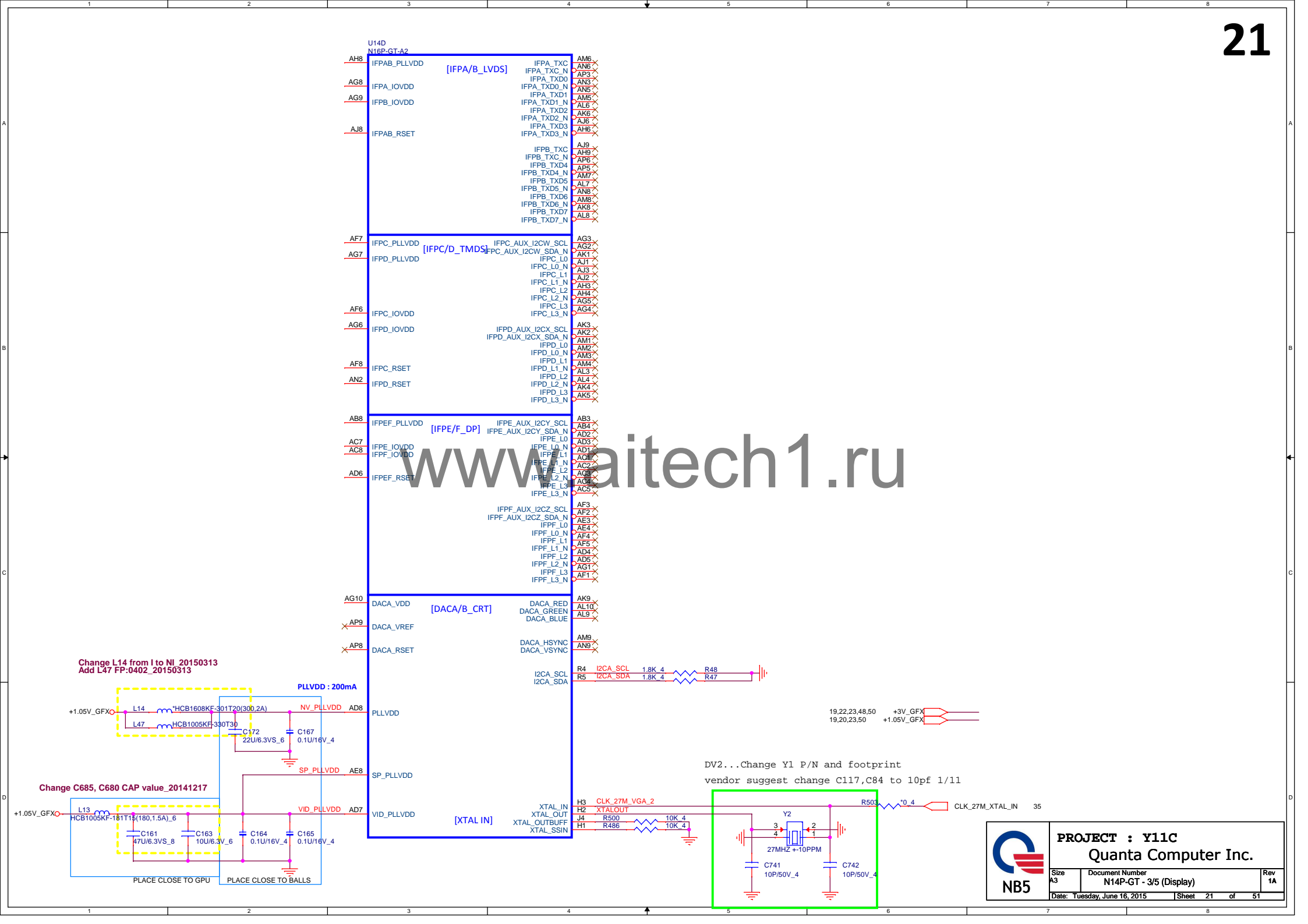
**Change L14 from I to NI\_20150313**  
Add L47 FP:0402\_20150313

**Change C685, C680 CAP value\_20141217**

**DV2...Change Y1 P/N and footprint**  
vendor suggest change C117,C84 to 10pf 1/11

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**U14D N14P-GT-A2**

**[IFPA/B\_LVDS]**

IFPA\_TXC, IFPA\_TXC\_N, IFPA\_TXD0, IFPA\_TXD0\_N, IFPA\_TXD1, IFPA\_TXD1\_N, IFPA\_TXD2, IFPA\_TXD2\_N, IFPA\_TXD3, IFPA\_TXD3\_N

**[IFPC/D\_TMDS]**

IFPC\_AUX\_I2C\_W\_SCL, IFPC\_AUX\_I2C\_W\_SDA\_N, IFPC\_L0, IFPC\_L0\_N, IFPC\_L1, IFPC\_L1\_N, IFPC\_L2, IFPC\_L2\_N, IFPC\_L3, IFPC\_L3\_N

**[IFPE/F\_DP]**

IFPE\_AUX\_I2C\_Y\_SCL, IFPE\_AUX\_I2C\_Y\_SDA\_N, IFPE\_L0, IFPE\_L0\_N, IFPE\_L1, IFPE\_L1\_N, IFPE\_L2, IFPE\_L2\_N, IFPE\_L3, IFPE\_L3\_N

**[DACA/B\_CRT]**

DACA\_RED, DACA\_GREEN, DACA\_BLUE, DACA\_HSYNC, DACA\_VSYNC

**[XTAL IN]**

XTAL\_IN, XTAL\_OUT, XTAL\_OUTB, XTAL\_SSIN

**Change L14 from I to NI\_20150313**  
**Add L47 FP:0402\_20150313**

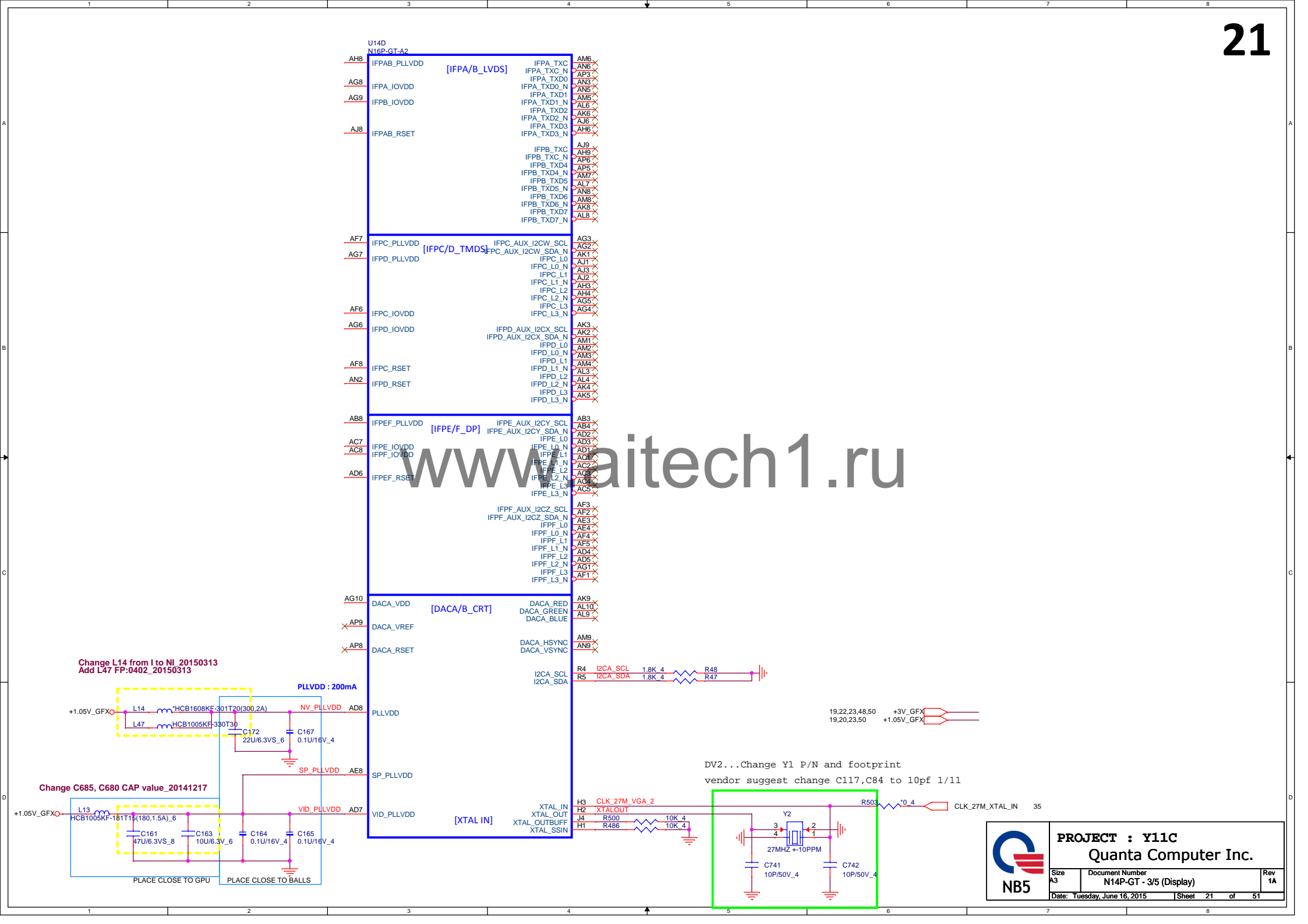
**Change C685, C680 CAP value\_20141217**

**PLLVDV : 200mA**

**DV2...Change Y1 P/N and footprint**  
**vendor suggest change C117,C84 to 10pf 1/11**

**PROJECT : Y11C**  
**Quanta Computer Inc.**

**Size A3**  
**Document Number N14P-GT - 3/5 (Display)**  
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**Rev 1A**





U14E  
N16P-GT-A2

[MIOA]

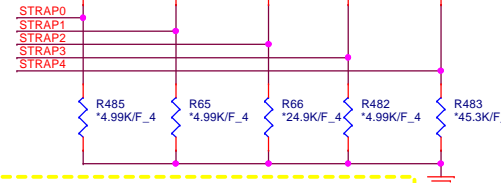
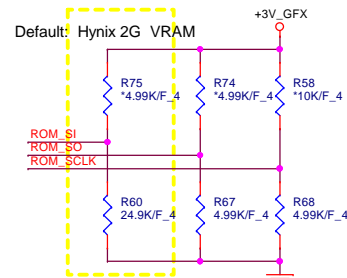
[MIOB]

[MISC\_GPIO/I2C/JTAG/THER]

[MISC2\_ROM]

MULTISTRAP\_REF\_GND

CEC



Latest Chocolate VRAM Table:

Default: Hynix 2G VRAM(Change to Micron)

N16P-GT device ID = 0x139A

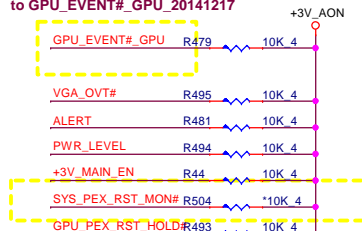
Vendor	TOP R/S QBC	Mfr. P/N	ROM_SI	H.P
Hynix (1.35V)	AKD5P2DTW01 AKD5P2DTW02	H5TC4G63CFR-N0C	0010 (0x4)	15K PD(R60)
Micron (1.35V)	AKD5P2STL00 AKD5P2STL01	MT41J256M16HA-093G:E	0100 (0x4)	24.9K PD(R60)
Samsung (1.35V)	AKD5PGDT500 AKD5PGDT501	K4W4G1646E-BC1A	0001 (0x1)	10K PD(R60)

Vendor	TOP R/S QBC	Mfr. P/N	ROM_SI	H.P
Hynix (1.35V)	AKD5PGWTW07 AKD5PGWTW08	H5TC4G63AFR-11C	0011 (0x3)	20K PD
Micron (1.35V)	AKD5P2STL00 AKD5P2STL01	MT41J256M16HA-093G:E	0100 (0x4)	24.9K PD
Samsung (1.35V)	AKD5PGWT502 AKD5PGWT501	K4W4G1646D-BC1A	0101 (0x5)	30.1K PD

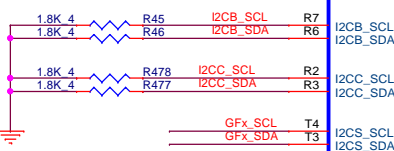
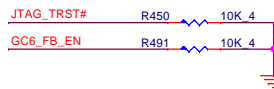
Netname	N16P-GT
ROM_SO	4.99K PD
ROM_SCLK	4.99K PD
STRAP0	49.9K PU
STRAP1	NC
STRAP2	NC
STRAP3	NC
STRAP4	NC

20150122 update VRAM

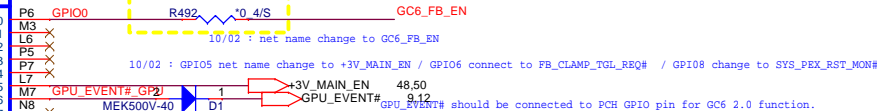
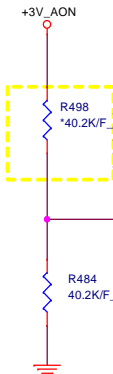
Change R492 from 0 to \*0.4/S 20150611

Change net name from GPU\_EVENT#  
to GPU\_EVENT#\_GPU\_20141217

Change R455 from I to NI\_20150109 (NV SCH)



Add R10779(NI) for SCH\_20141217



10/02 : GPIO5 net name change to +3V\_MAIN\_EN / GPIO6 connect to FB\_CLAMP\_TGL\_REQ# / GPIO8 change to SYS\_PEX\_RST\_MON#

MEK500V-40 D1 GPU\_EVENT# should be connected to PCH GPIO pin for GC6 2.0 function.

GPU\_EVENT# 9.12

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GPU\_EVENT# 9.12

GPU\_EVENT# 9.12

GPU\_EVENT# 9.12

4.99K/F\_4: CS24992FB26 RES CHIP 4.99K 1/16W +1% (0402)  
 10K/F\_4: CS31002FB26 RES CHIP 10K 1/16W +1% (0402)  
 15K/F\_4: CS31502FB24 RES CHIP 15K 1/16W +1% (0402)  
 20K/F\_4: CS32002FB29 RES CHIP 20K 1/16W +1% (0402)  
 24.9K/F\_4: CS32492FB16 RES CHIP 24.9K 1/16W +1% (0402)  
 30.1K/F\_4: CS33012FB18 RES CHIP 30.1K 1/16W +1% (0402)  
 34.8K/F\_4: CS33482FB22 RES CHIP 34.8K 1/16W +1% (0402)  
 45.3K/F\_4: CS34532FB18 RES CHIP 45.3K 1/16W +1% (0402)

Logical Strap Bit Mapping

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Table 15-4 GB3-256 Multi-Level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GE[3]	PCIE_MAX_SPEED	DP_PLL_VDD3V

Table 6. N16P-GT DDR3L Recommended Memories

Memory Type	FBVDD/FBVDQ	Memory Density	Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
DDR3L	1.35V/1.35V	128Mb	Single Rank	Hynix	H5TC263FR-11C	F-die	0x9	900	N/A	Production candidate
				Micron	MT41J128M16JT-093G:K	K-die	0xA	900	1322	Production candidate
				Samsung	K4W2G1646Q-BC1A	Q-die	0xB	900	N/A	Production candidate
	1.35V/1.35V	256Mb	Single Rank	Hynix	H5TC463AFR-11C	A-die	0x9	900	N/A	Production candidate
				Micron	MT41J256M16HA-093G:E	E-die	0xA	900	1322	Production candidate
				Samsung	K4W4G1646D-BC1A	D-die	0xB	900	N/A	Production candidate

Hynix  
SamsungC die 0x2  
E die 0x1

GPIO ASSIGNMENTS

GPIO	SM107/GMT08	GK208/GK107
GPIO0	GCS_FB_EN	GPIO_FB_CLAMP
GPIO1	MEM_VDD_CTL	MEM_VDD_CTL
GPIO2	LCD_BL_PWM	LCD_BL_PWM
GPIO3	LCD_PWR_EN	LCD_PWR_EN
GPIO4	LCD_BL_EN	LCD_BL_EN
GPIO5	GCS_PWR_EN	DEBUG SERVICE HEADER
GPIO6	GPU_EVENT#	Remote Sensor Error Correction
GPIO7	DEBUG SERVICE HEADER	3D STEREO
GPIO8	SYS_PEX_RST_MON#	GPU OVERTEMP
GPIO9	Remote Sensor Error Correction	GPU THERMAL_ALERT/FAN_PWM
GPIO10	MEM_VREF_CTL(N/A)	MEM_VREF_CTL(N/A)
GPIO11	NVDDO_PWM_VDD	NVDDO_PWM_VDD
GPIO12	AC DETECT	AC DETECT
GPIO13	NVDDO_PSI	NVDDO_PSI
GPIO14	IFPG_HDP	N/C
GPIO15	N/C	N/C
GPIO16	FRAME LOCK	FRAME LOCK
GPIO17	IFPD_HDP(OP1M)	IFPD_HDP(OP1M)
GPIO18	IFPE_HDP(OP1M)	IFPE_HDP(OP1M)
GPIO19	IFPF_HDP(OP1M)	IFPF_HDP(OP1M)
GPIO20	GCS_MODE	N/A
GPIO21	GPU_PEX_RST_HOLD#	N/A

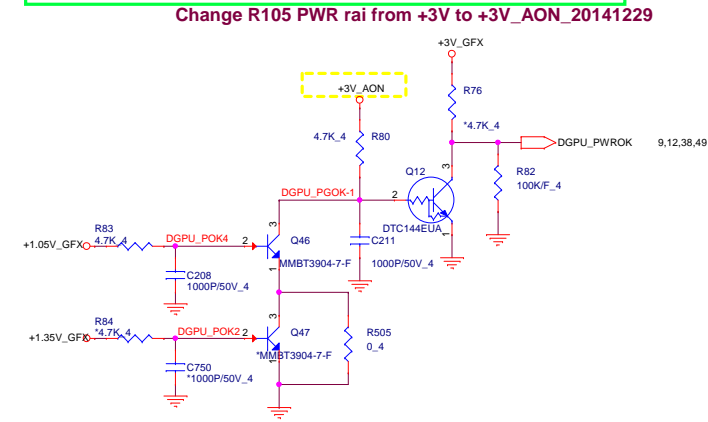
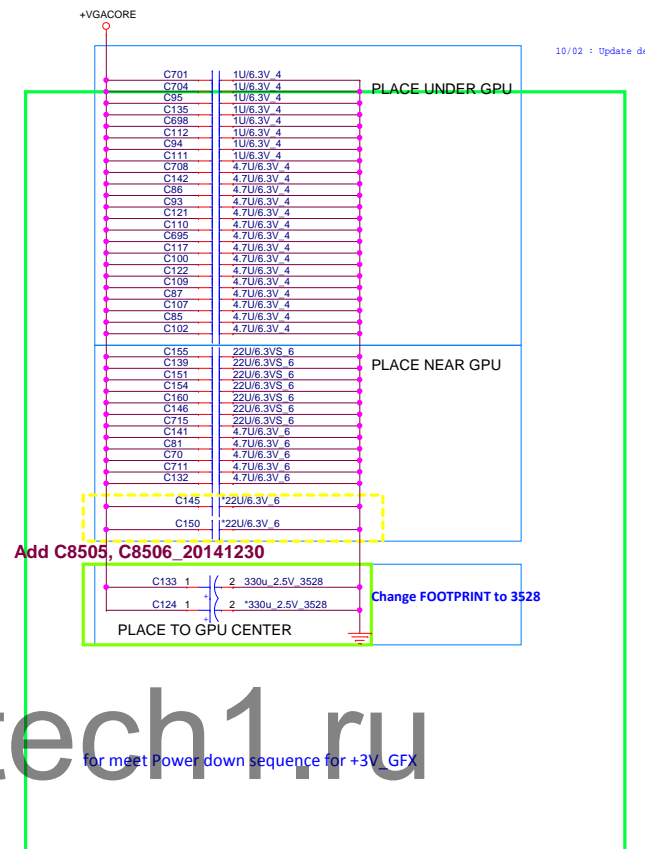
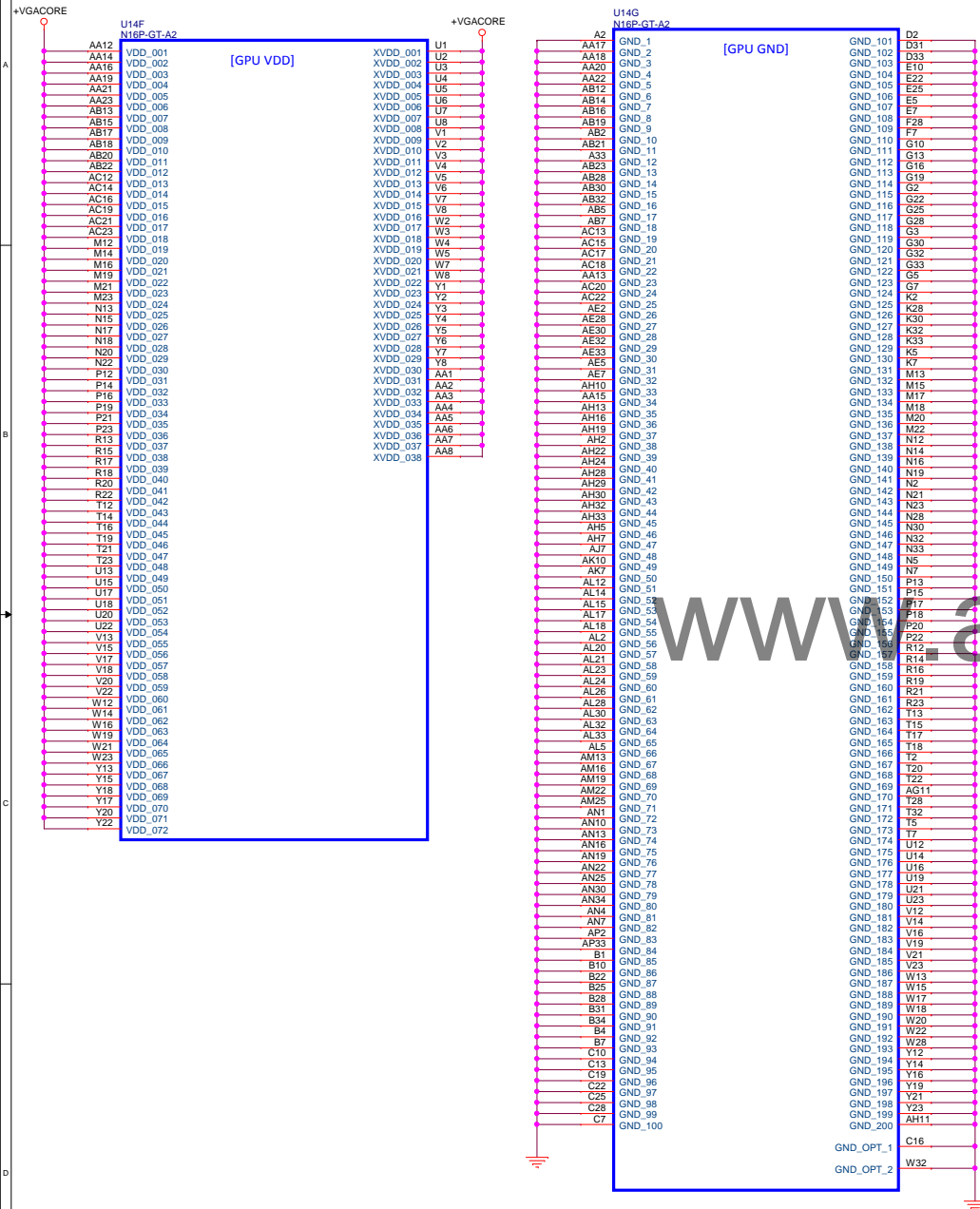


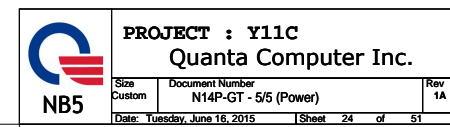
PROJECT : Y11C  
 Quanta Computer Inc.

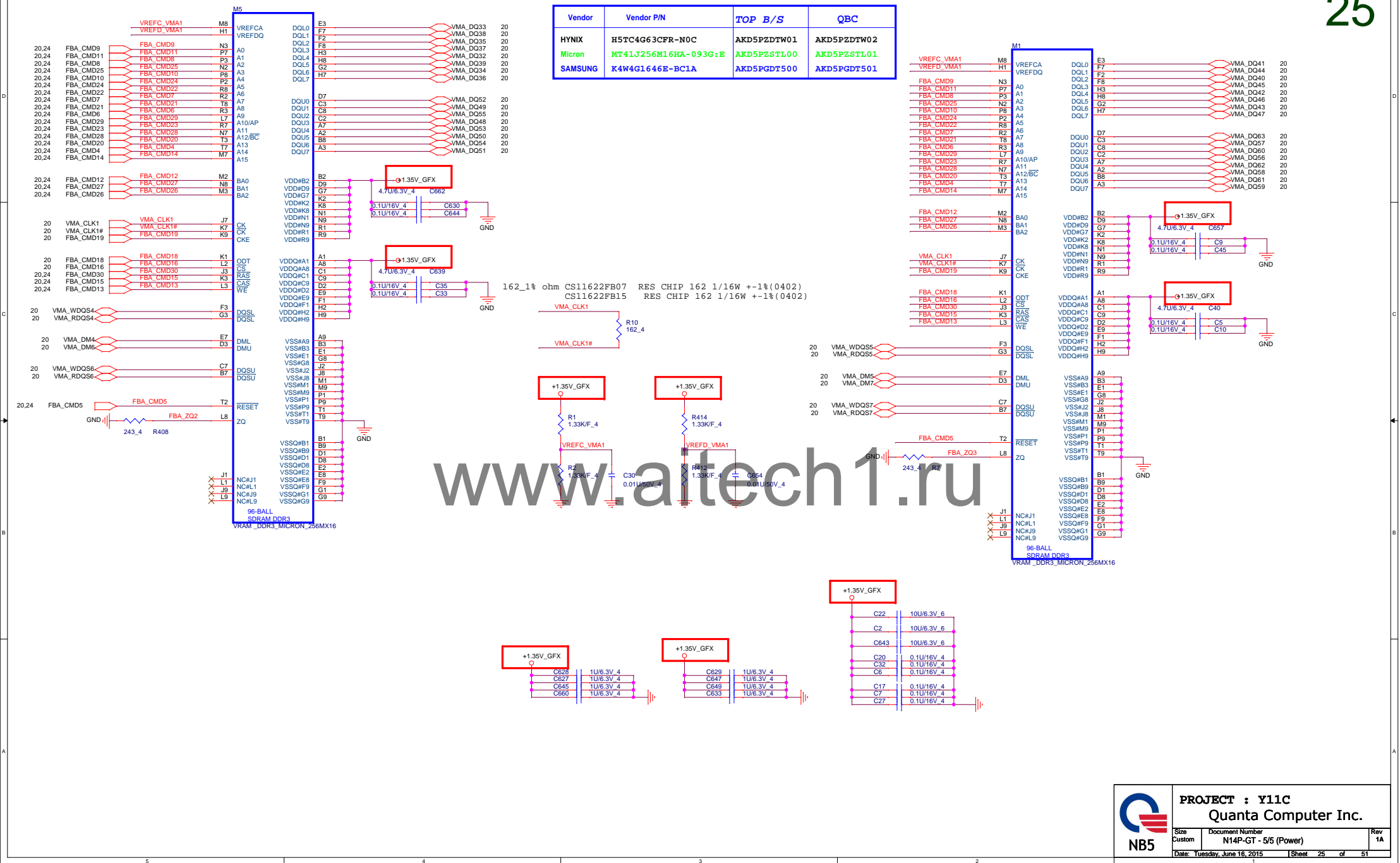
Size	Document Number	Rev
Custom	N14P-GT - 4/5 (MISC)	1A
Date: Tuesday, June 16, 2015	Sheet 22 of 51	



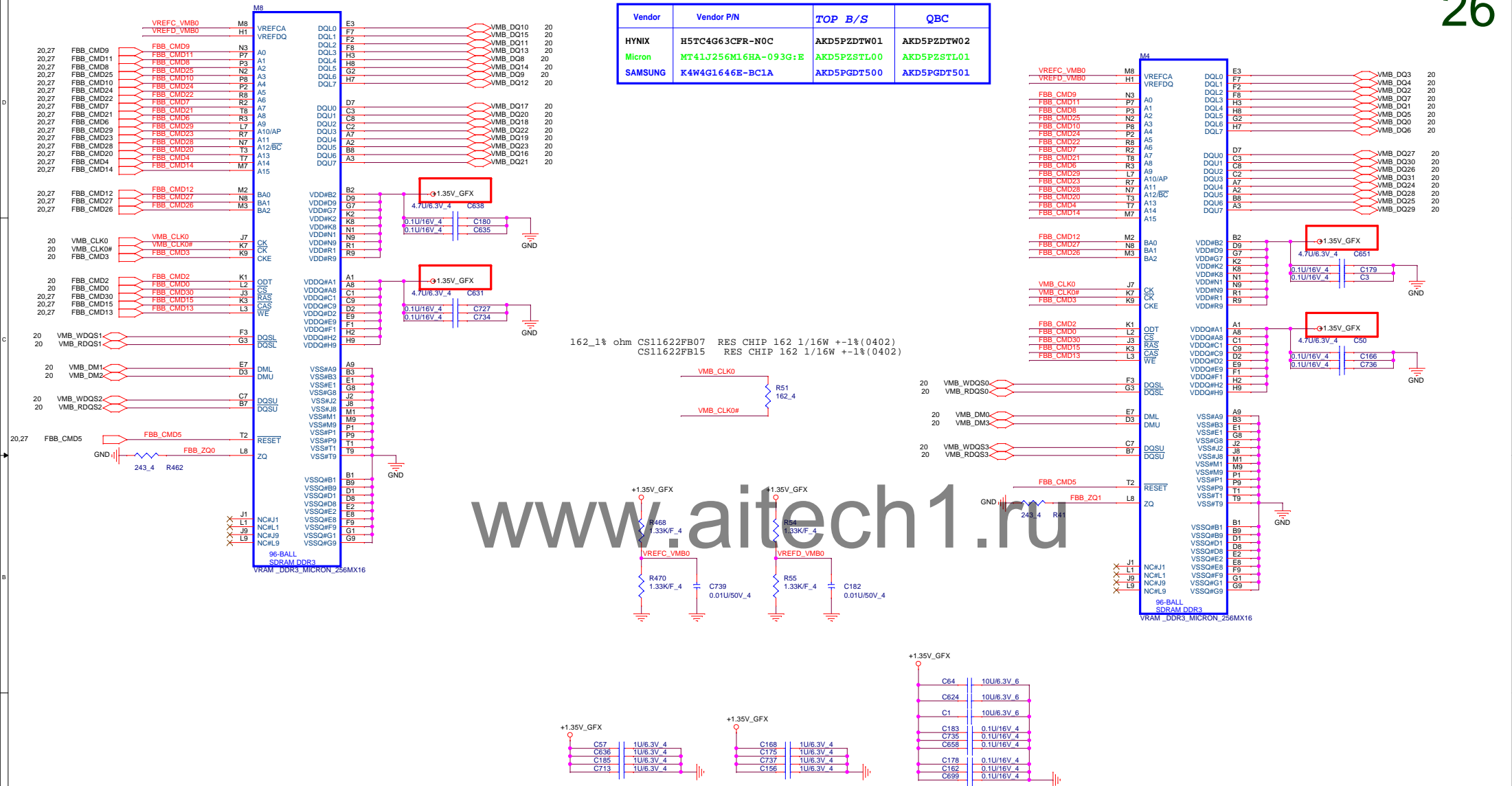
VDD/XVDD : 25.72A



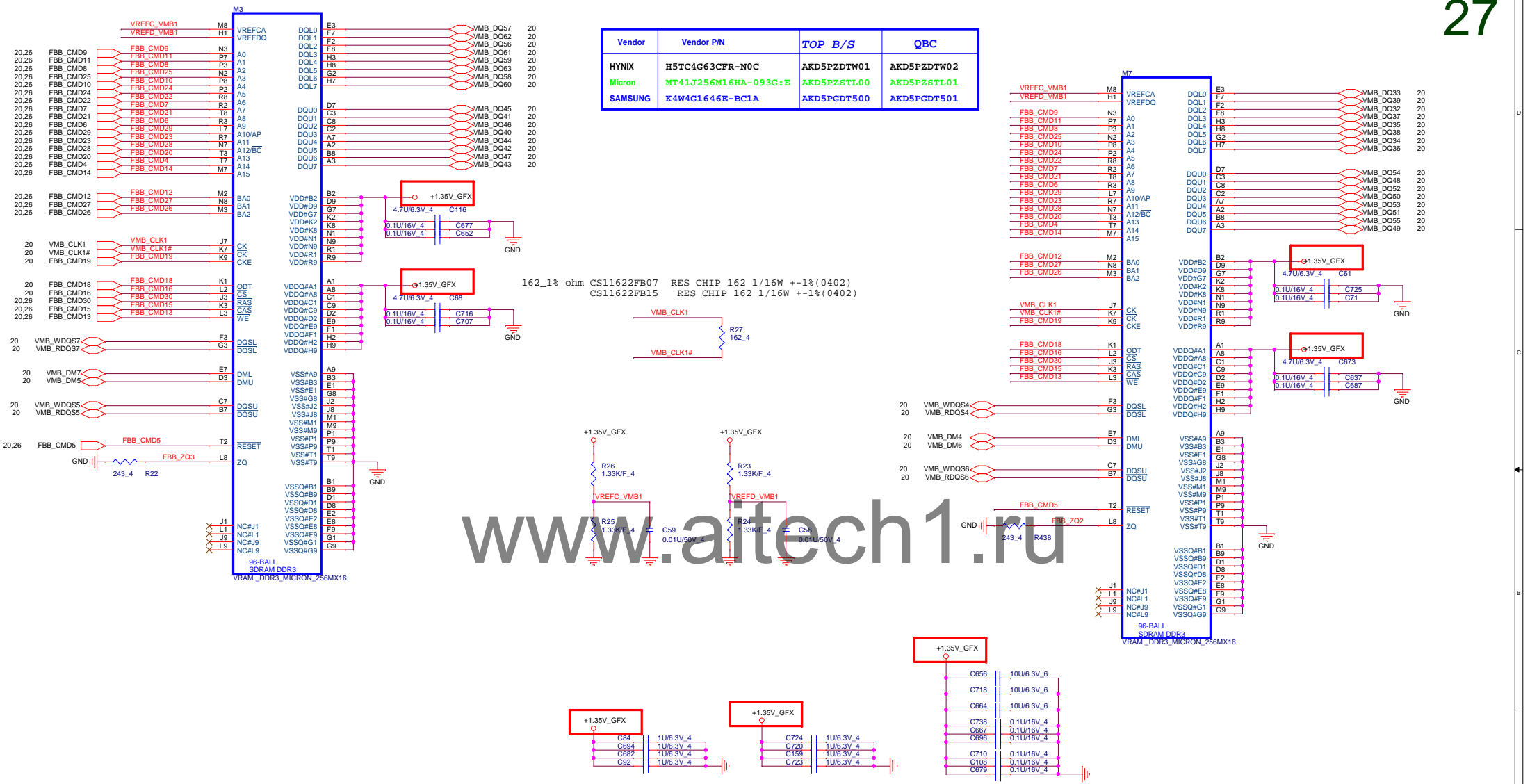




Vendor	Vendor P/N	TOP E/S	QBC
HYNIX	H5TC4G63CFR-N0C	AKD5P2DWTW01	AKD5P2DWTW02
Micron	MT41L7256M16HA-093G:E	AKD5P2STL00	AKD5P2STL01
SAMSUNG	K4W4G1646E-BC1A	AKD5PGDT500	AKD5PGDT501



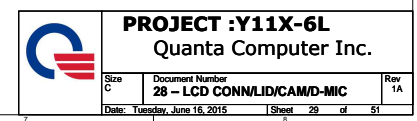
Vendor	Vendor P/N	TOP B/S	QBC
HYNIX	H5TC4G63CFR-N0C	AKD5PZDTW01	AKD5PZDTW02
Micron	MT41J256M16HA-093G:E	AKD5PZSTL00	AKD5PZSTL01
SAMSUNG	K4W4G1646E-BC1A	AKD5PGDT500	AKD5PGDT501

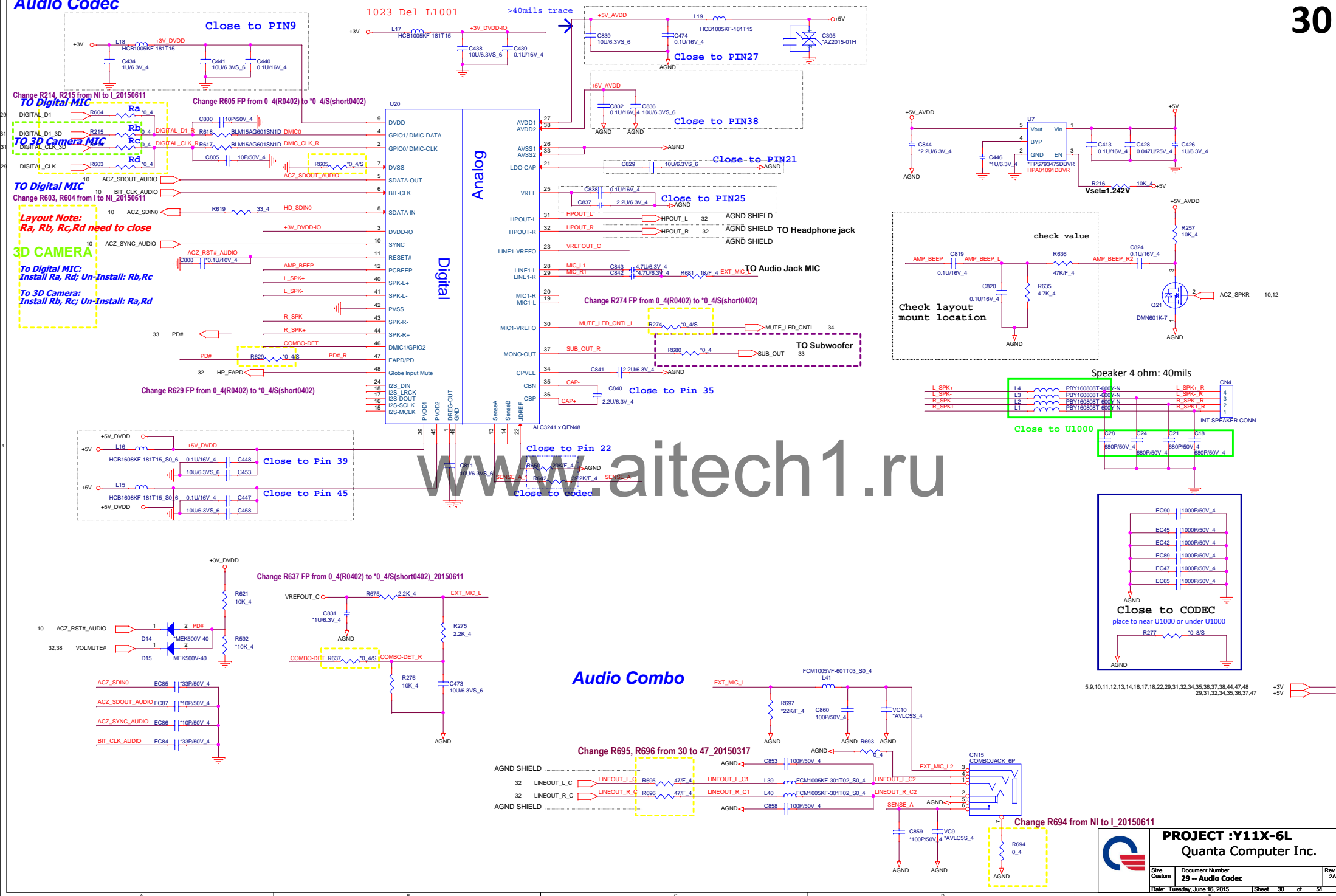


Del DP to LVDS IC\_20150310

[www.aitech1.ru](http://www.aitech1.ru)



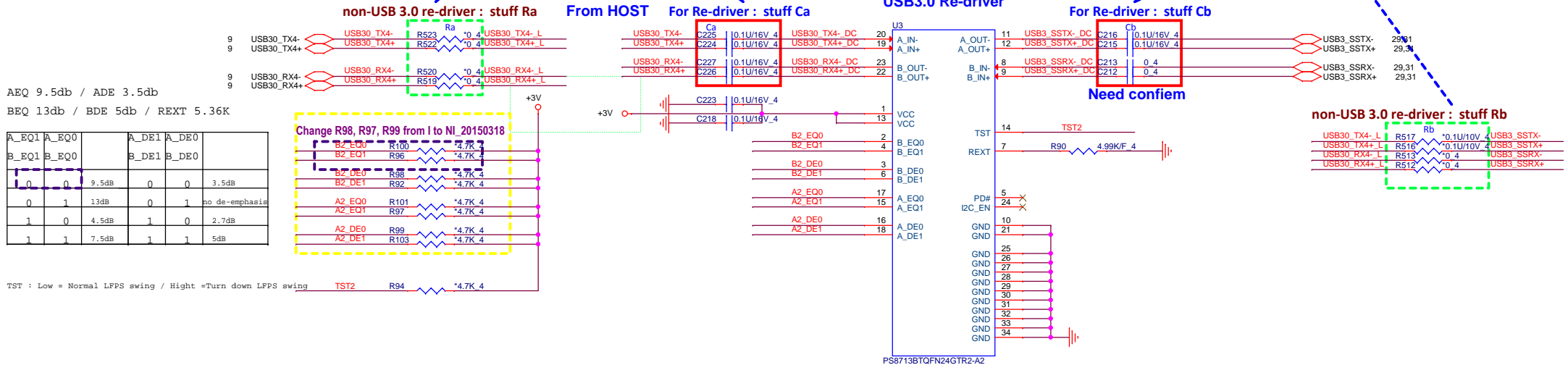
**LVDS Conn.**



# USB 3.0 re-driver for 3D Camera

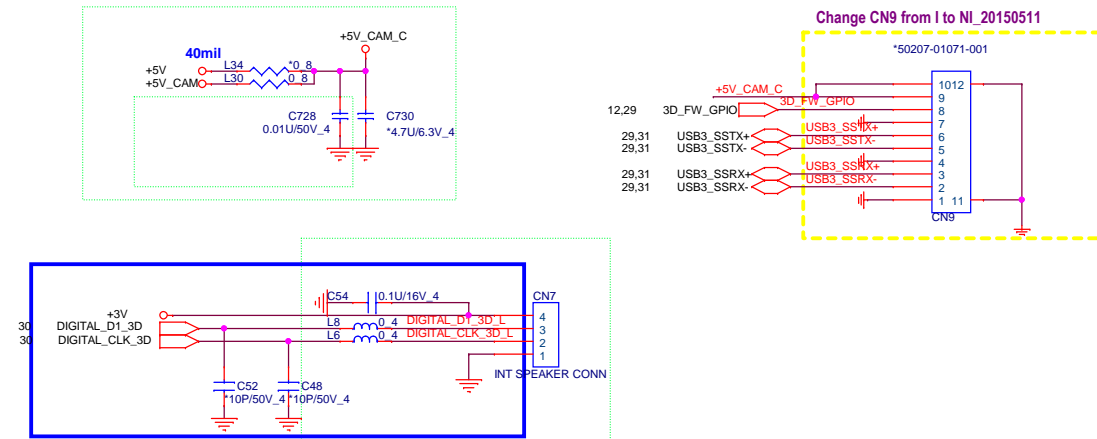
31

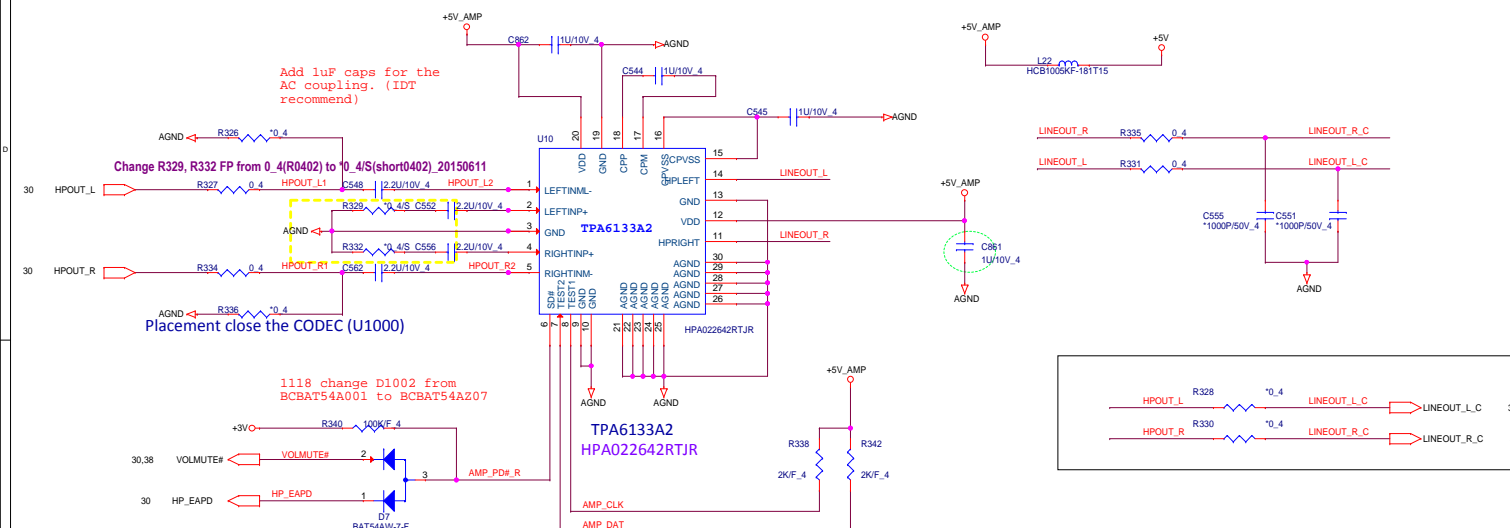
## 3D Camera CON & USB3 re-driver for 3D.



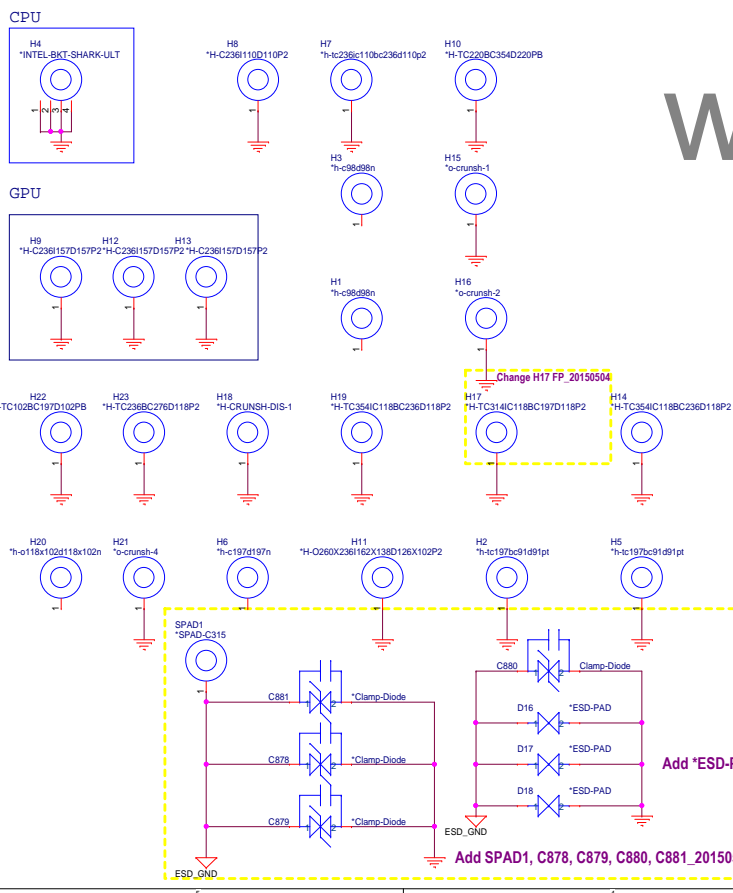
www.aitech1.ru

### 3D Camera Conn.

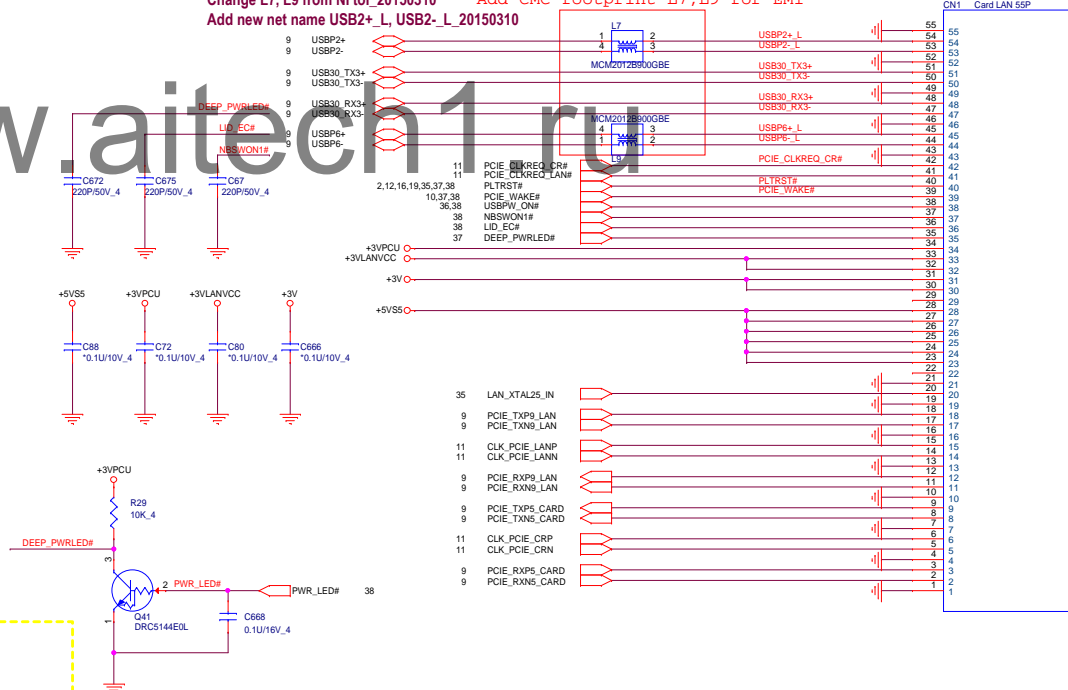




## HOLE



Change L7, L9 from NI to 20150310 Add CMC footprint L7, L9 for EMI  
Add new net name USB2+\_L, USB2-\_L 20150310



**PROJECT :Y11X-6L**  
**Quanta Computer Inc.**

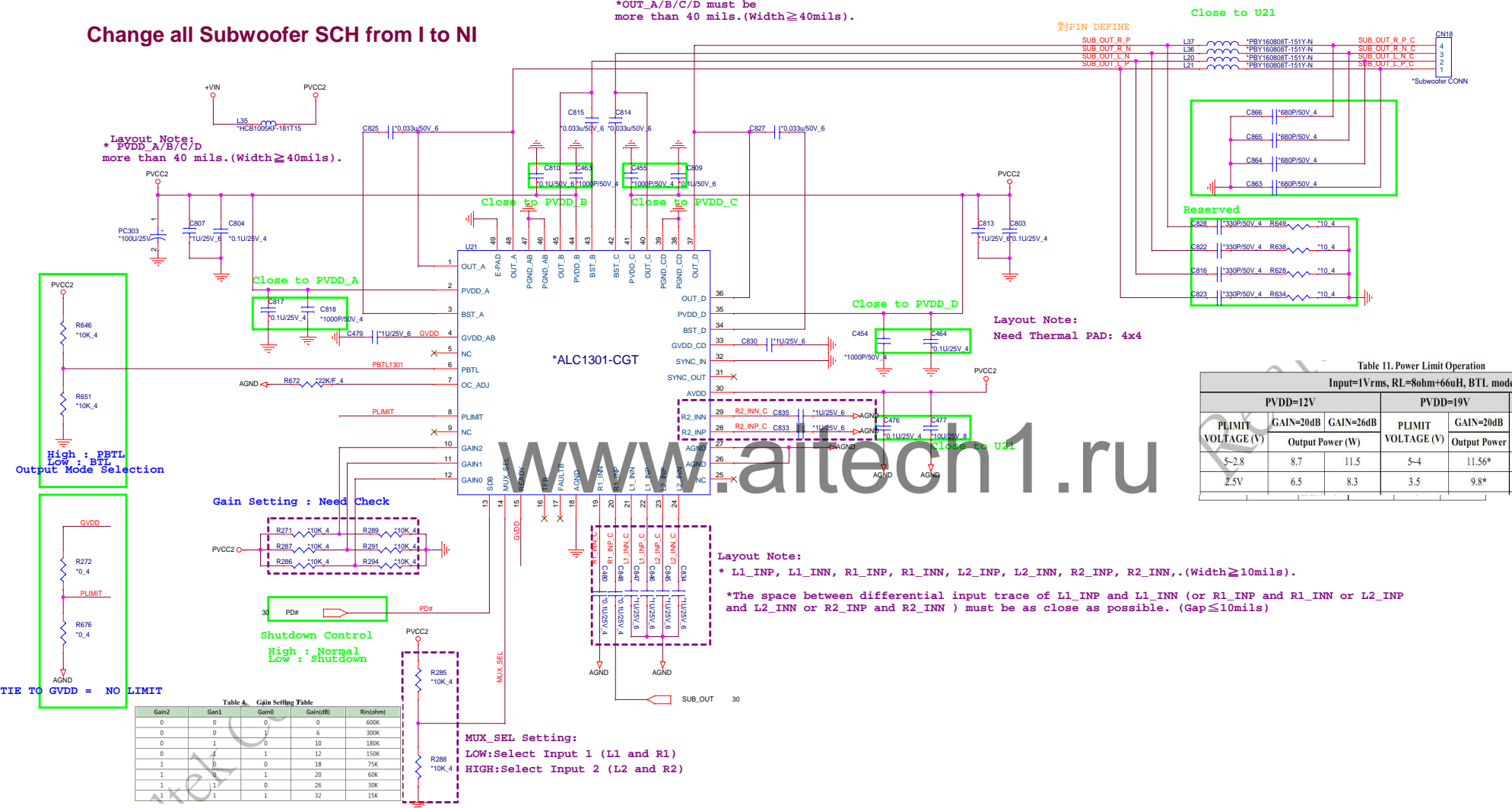
Size C Document Number  
**30 - Card Reader**  
Date: Tuesday, June 16, 2015 Sheet 32 of 51

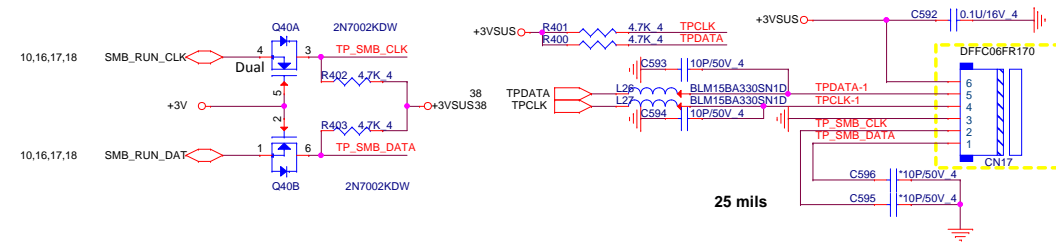
## For Power Crunch 15" Subwoofer

Change all Subwoofer SCH from I to NI

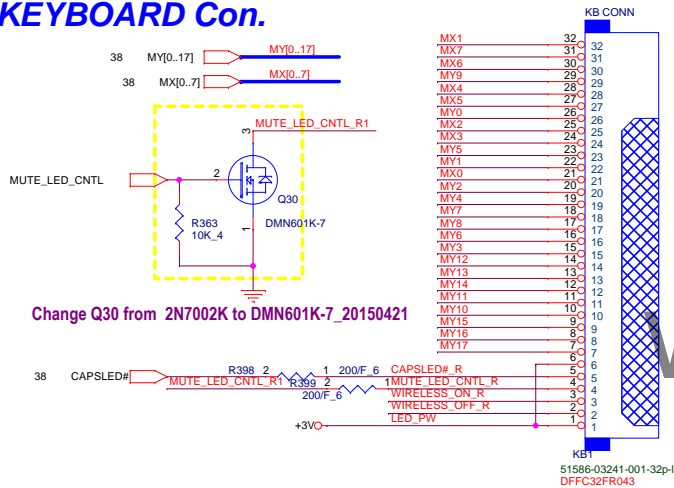
## Layout Note:

\*The space between differential output trace of OUT\_A and OUT\_B (or OUT\_C and OUT\_D) must be as close as possible. ( $\leq 10\text{mils}$ )  
 \*OUT\_A/B/C/D must be more than 40 mils. (Width  $\geq 40\text{mils}$ ).

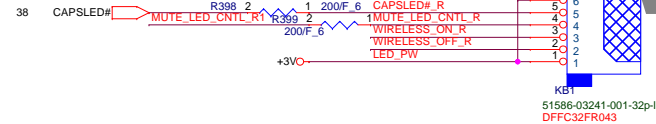




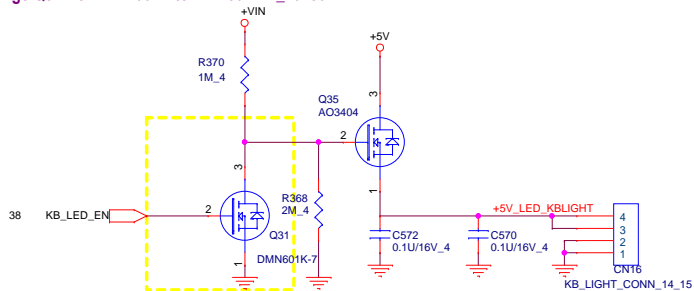
## KEYBOARD Con.



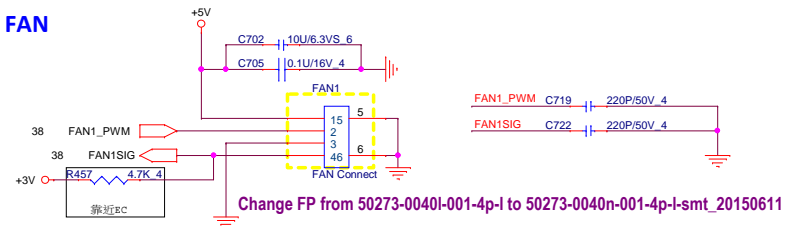
Change Q30 from 2N7002K to DMN601K-7\_20150421



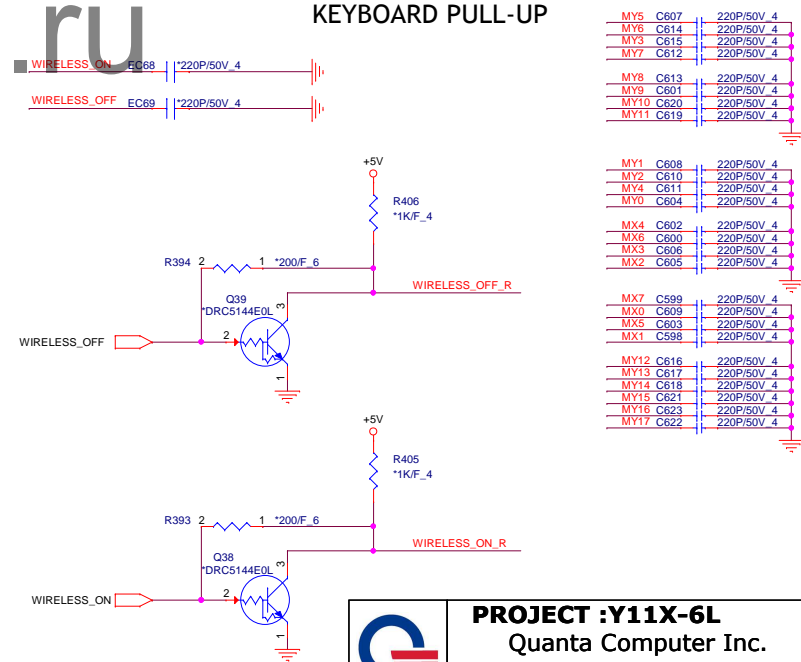
Change Q31 from 2N7002K to DMN601K-7\_20150421



## FAN



## KEYBOARD PULL-UP



**PROJECT :Y11X-6L**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	31 - PB/TP/KB/FAN/EMI Cap	1A
Date: Tuesday, June 16, 2015	Sheet 34 of 51	

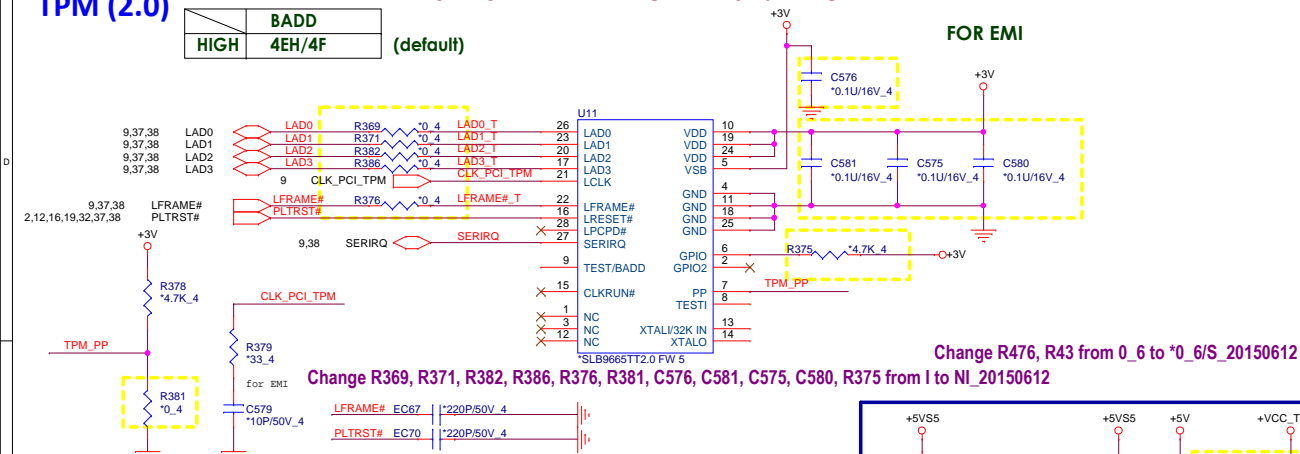


## TPM (2.0)

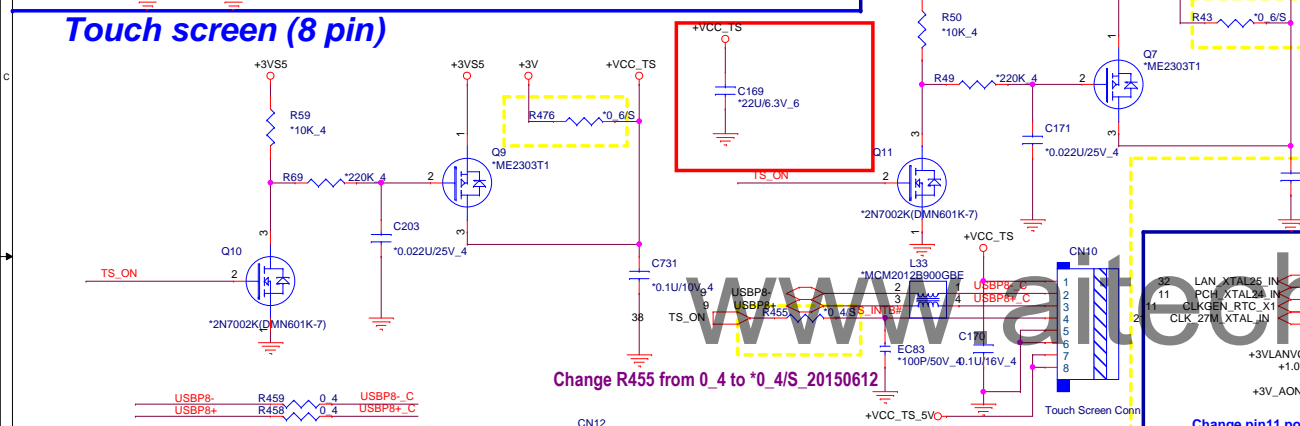
	<b>BADD</b>
<b>HIGH</b>	<b>4EH/4F</b> (default)

## CHECK DB TPM INSTALL or un-INSTALL

FOR EMI



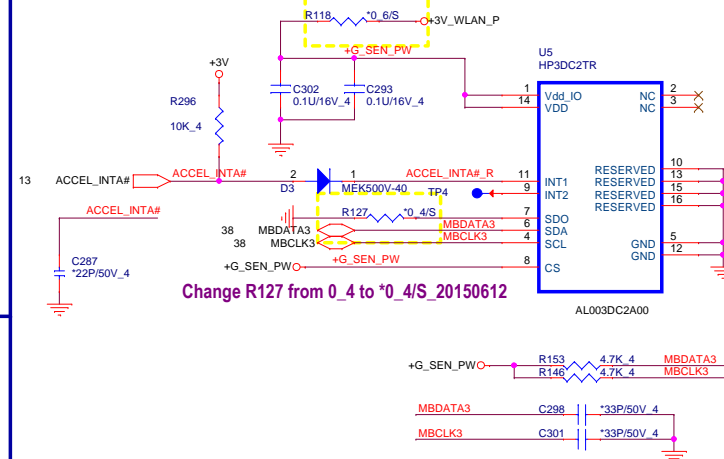
***Touch screen (8 pin)***



## Accelerometer Sensor

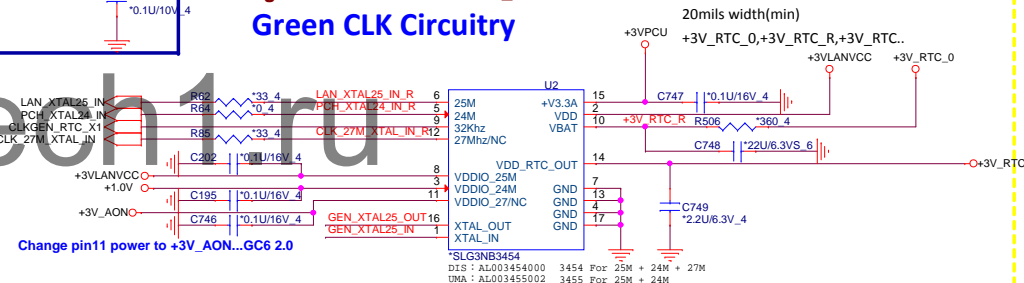
Change R118 from 0\_6 to \*0\_6/S\_20150612

**G-Sensor Power need check**

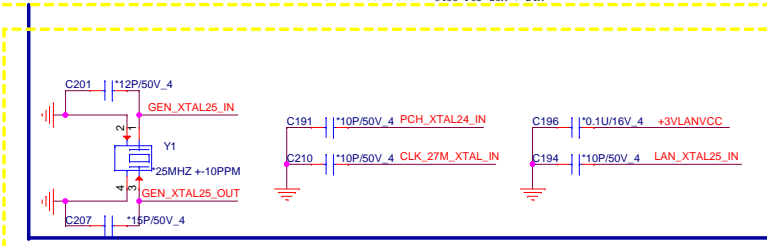
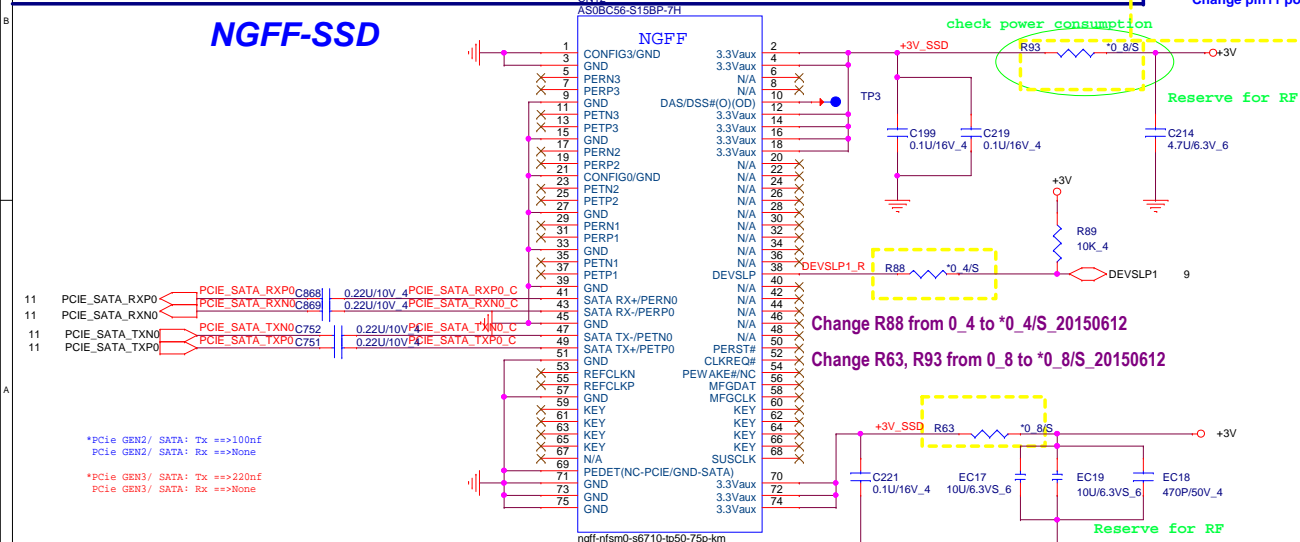


**Change Green CLK from I to NI\_20150129**

## Green CLK Circuitry



## NGFF-SSD

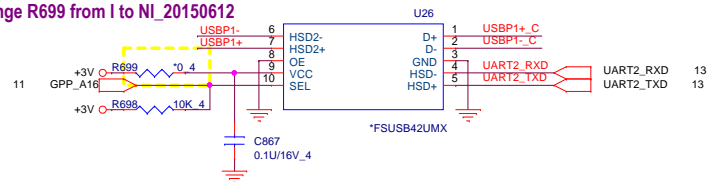


**PROJECT :Y11X-6L**  
Quanta Computer Inc.

Size Custom	Document Number <b>32 -- TPM/G-Sensor/G-CLK/TS/FP</b>	Rev 1A
Date: Tuesday, June 16, 2015	Sheet 35 of 51	

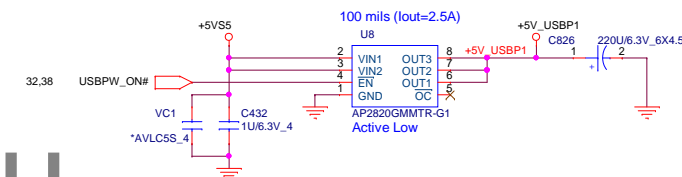
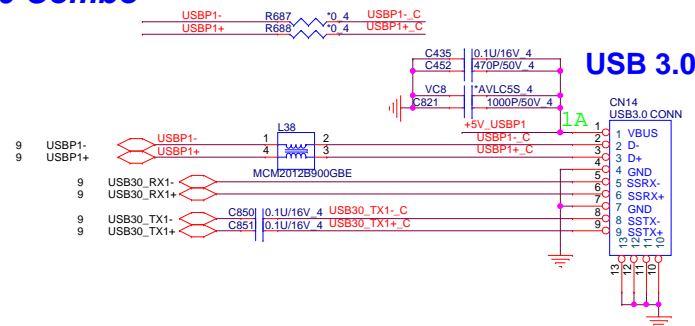
## UART for DEBUG

Change R699 from I to NI\_20150612



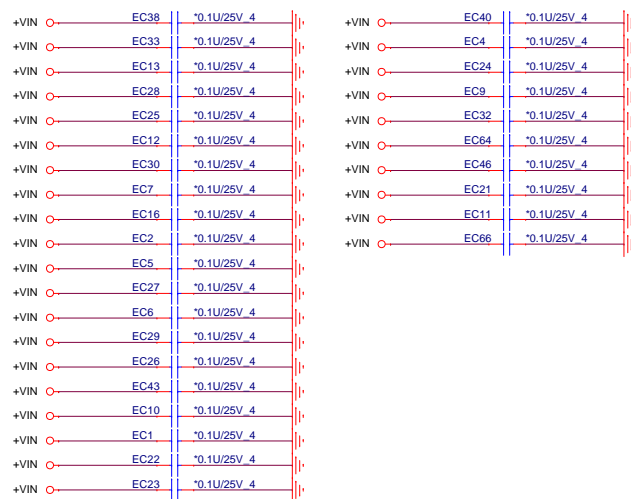
Change R455 from 0\_4 to \*0\_4/S\_20150612

## USB 2.0/3.0 Combo

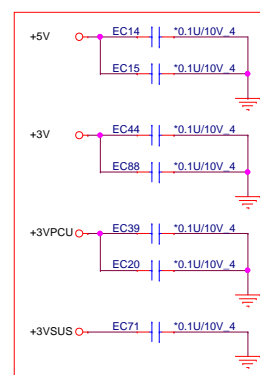


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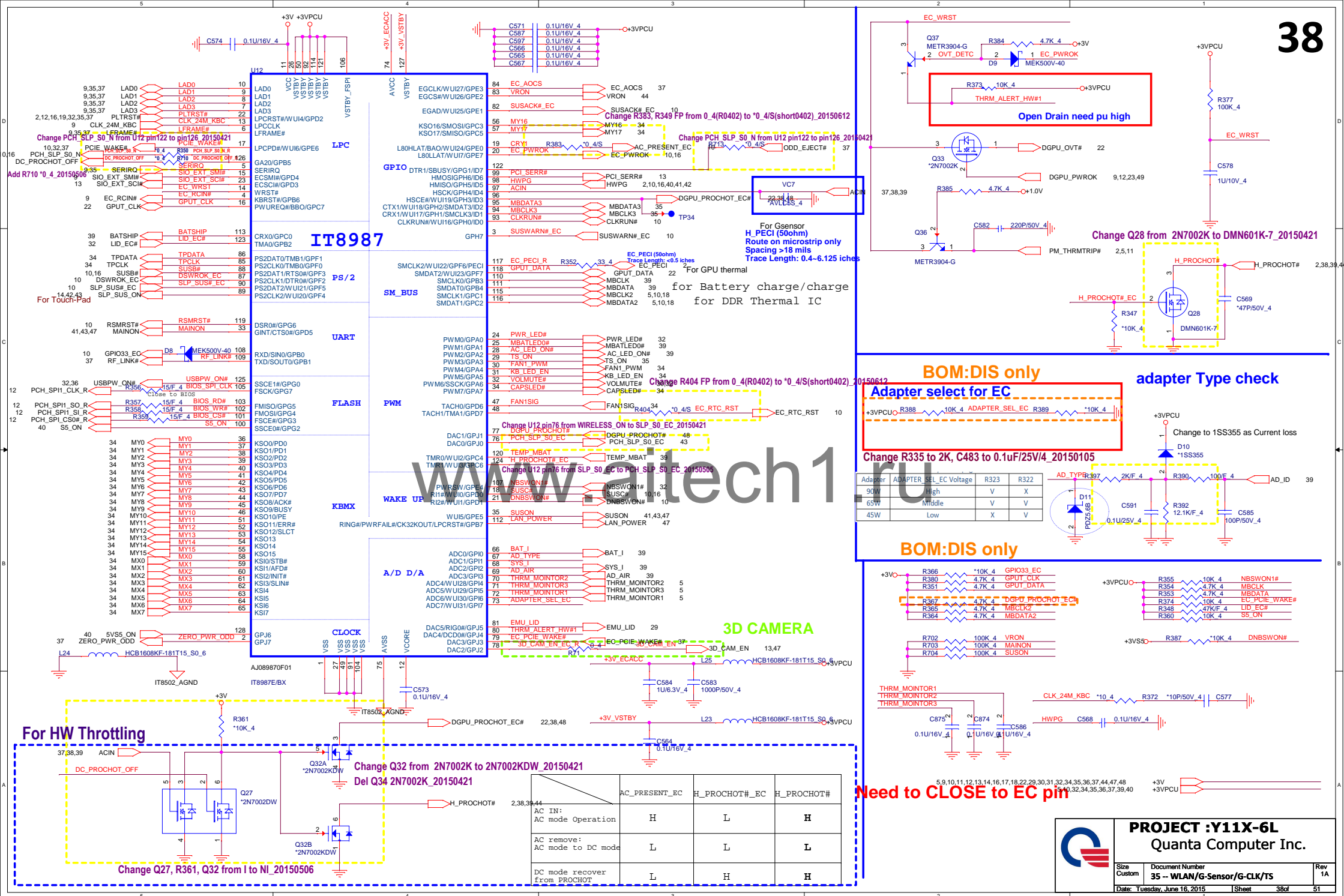
# EMI CAP

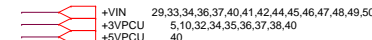


## Reserve EMI CAP



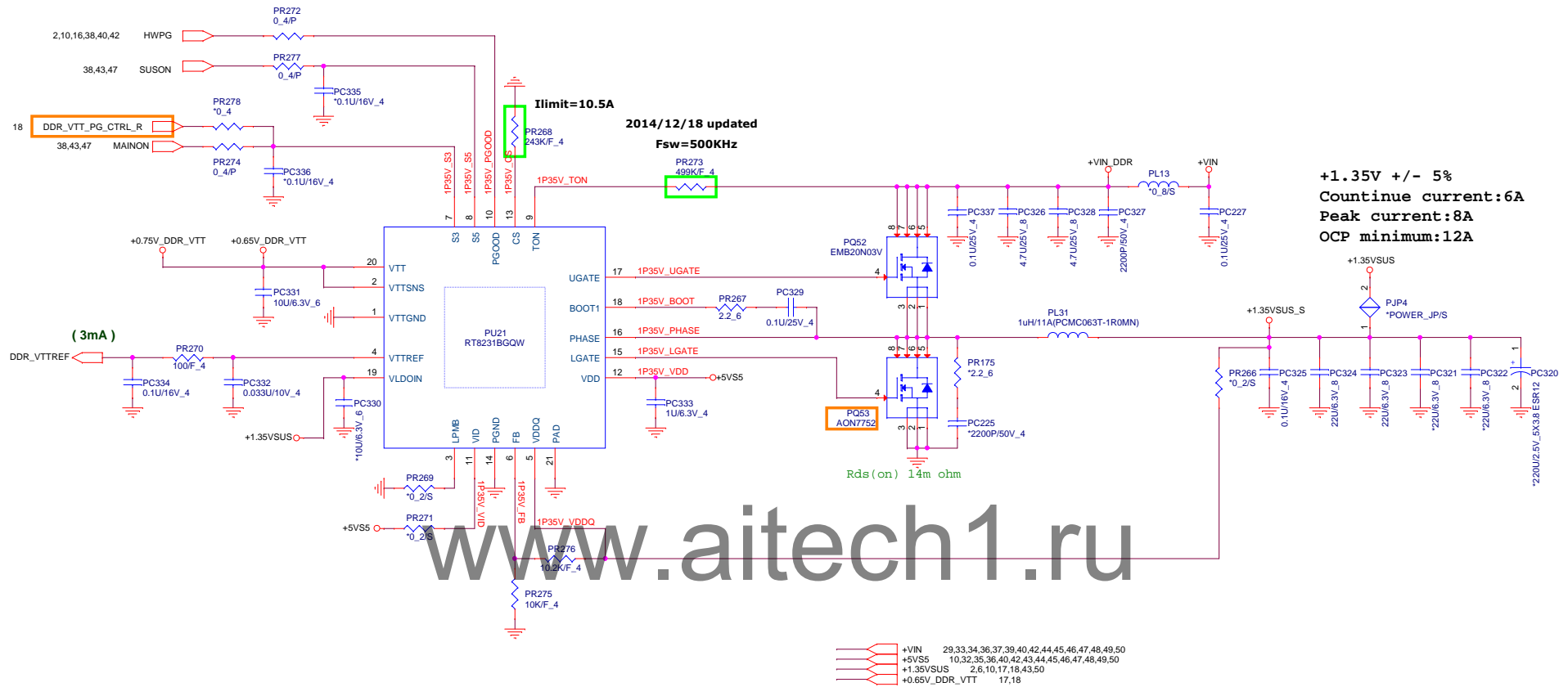


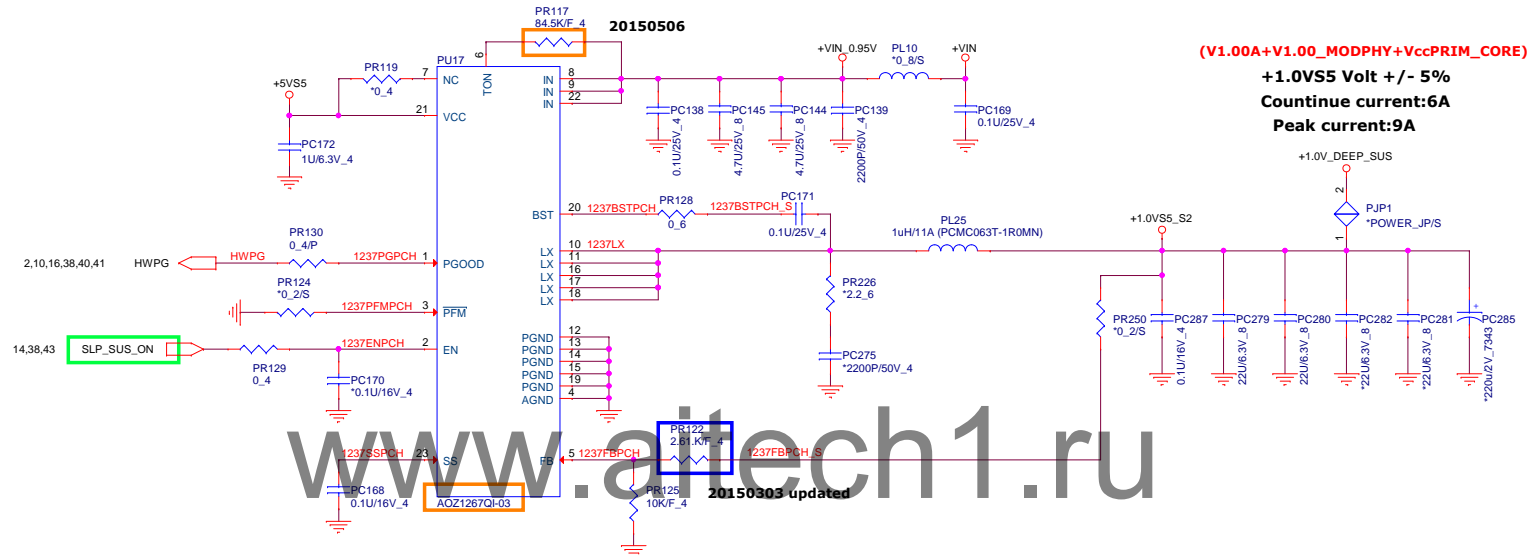




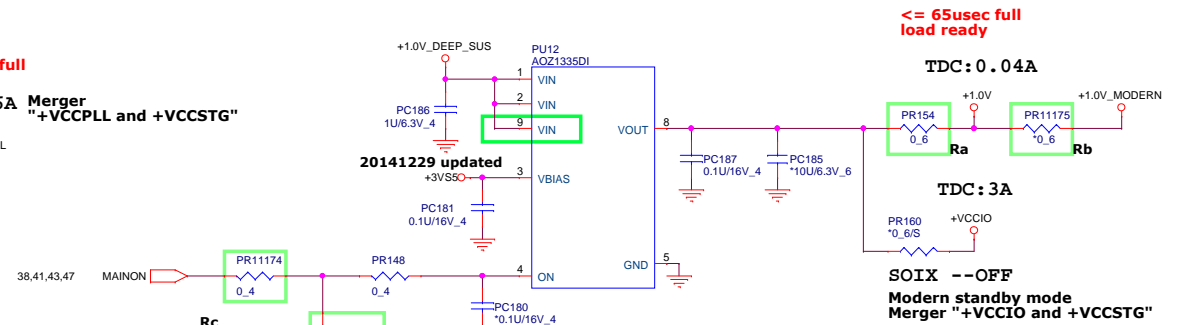
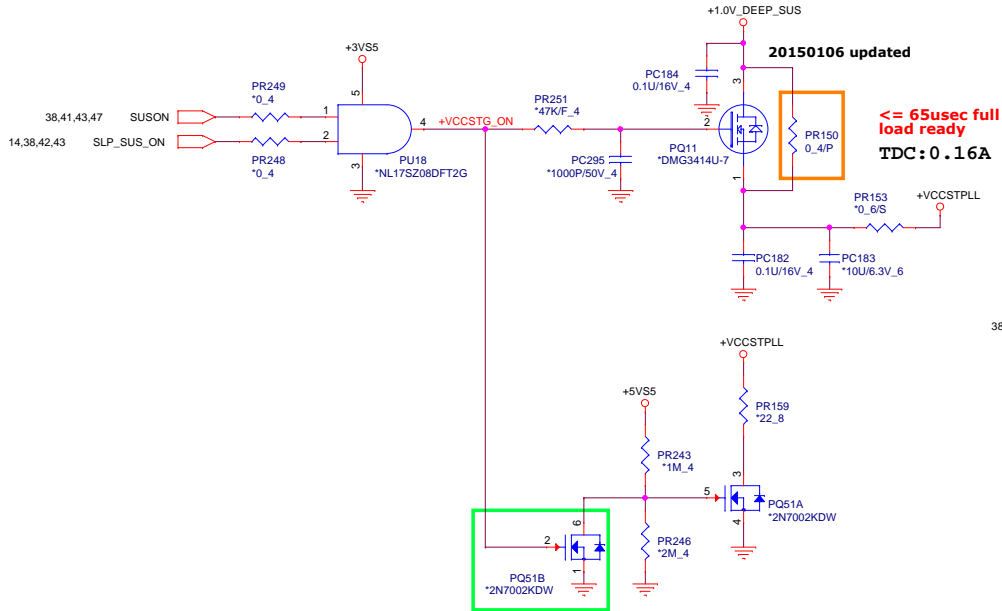








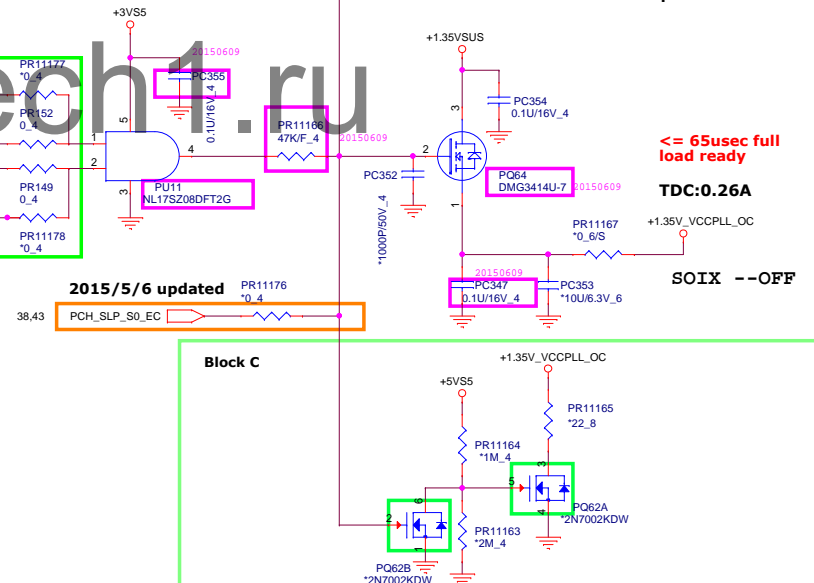
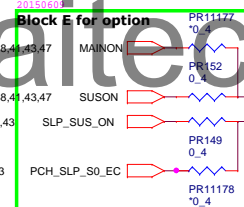
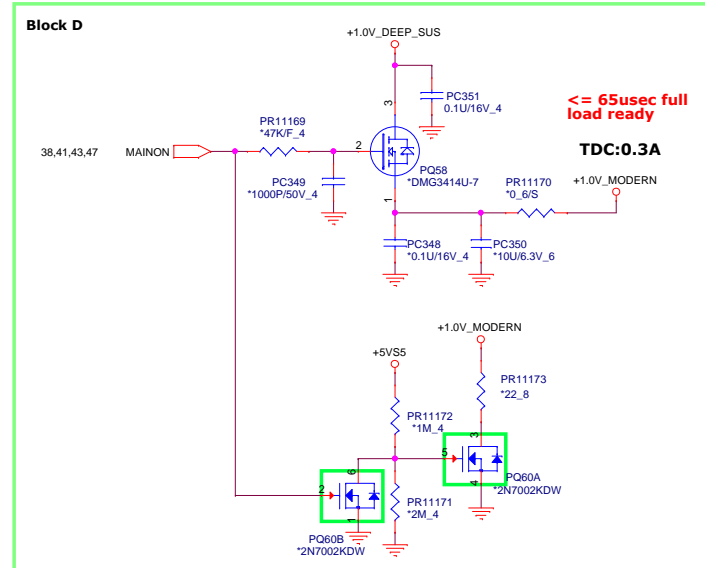
+1.0V 2,5,6,10,16,35,38  
 +3VS5 10,12,14,16,35,37,38,40,47,50  
 +5VS5 10,32,35,36,40,41,42,44,45,46,47,48,49,50  
 +VCCIO 3,6,16  
 +VCCSTPLL 2,6,44  
 +1.0V\_DEEP\_SUS 10,11,14,16,42



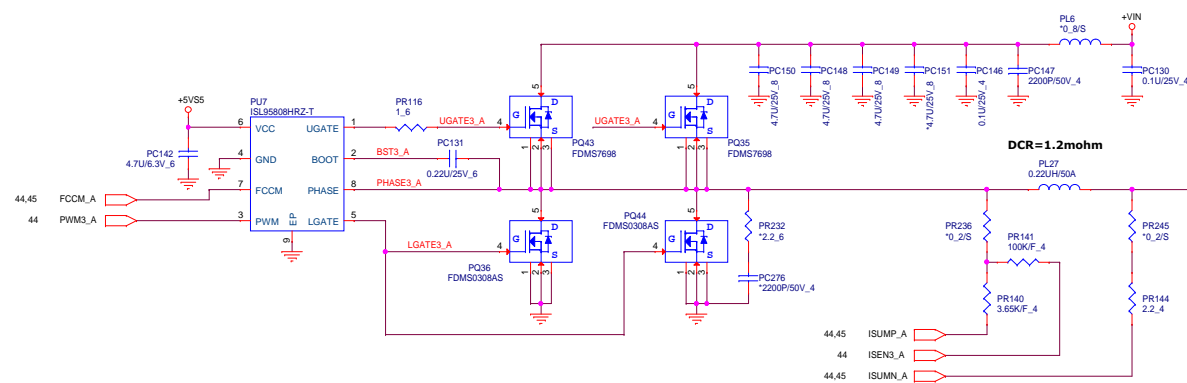
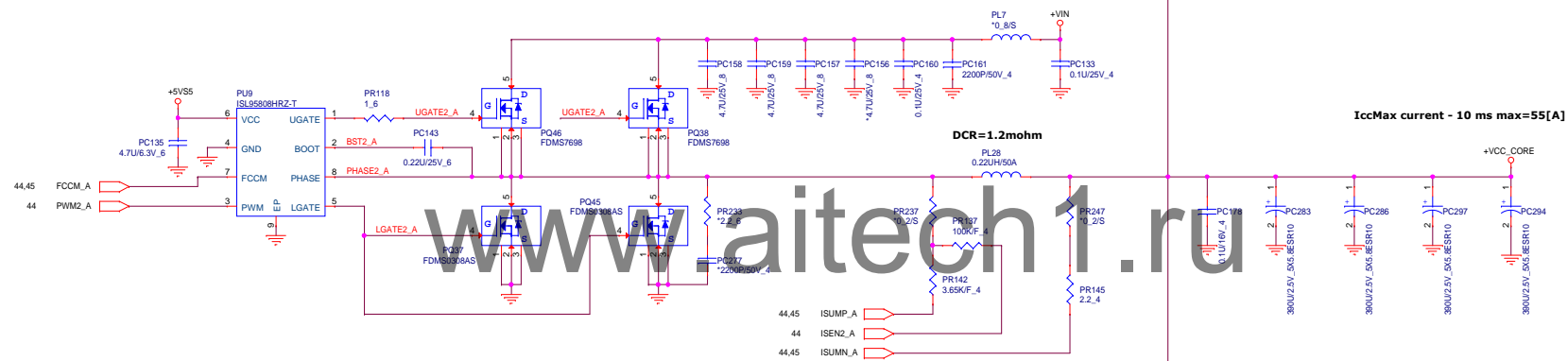
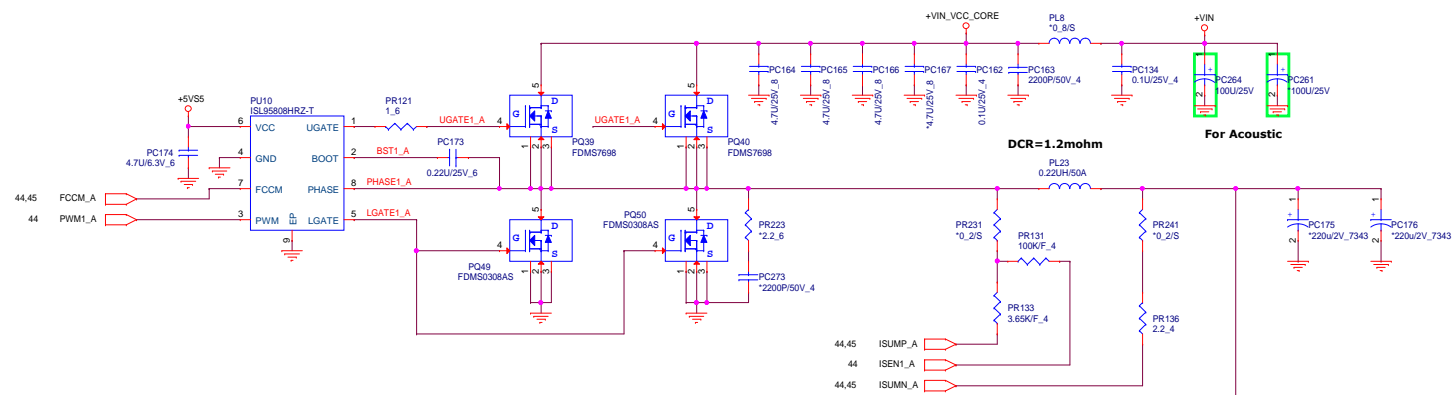
**Support Modern standby mode**

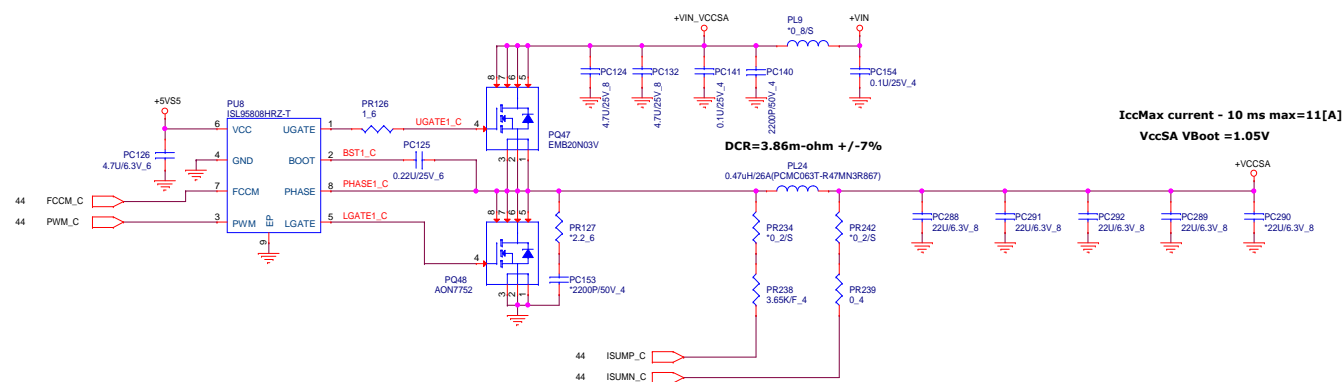
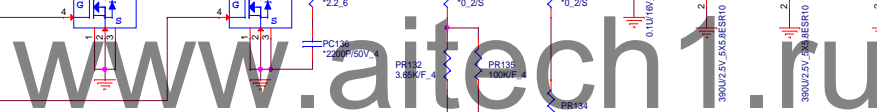
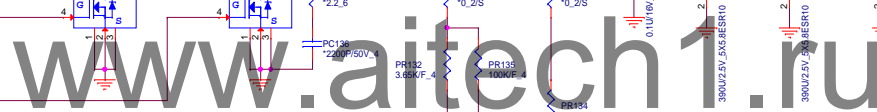
1. Remove Ra/Rc & stuff Rb/Rd
2. stuff block C & D
3. Block E for option

**Reserve for Modern StandBy**



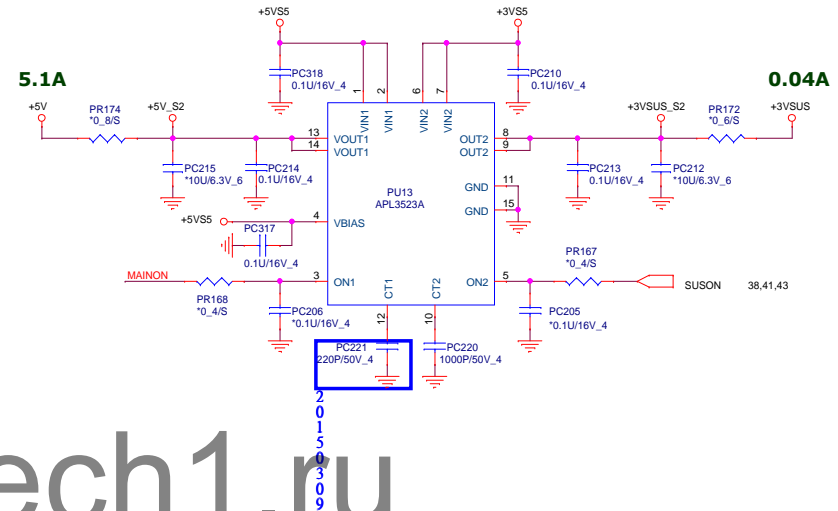
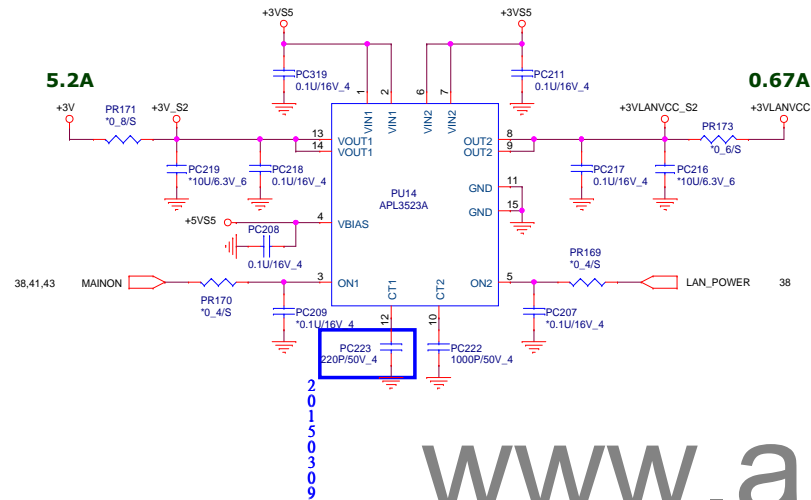




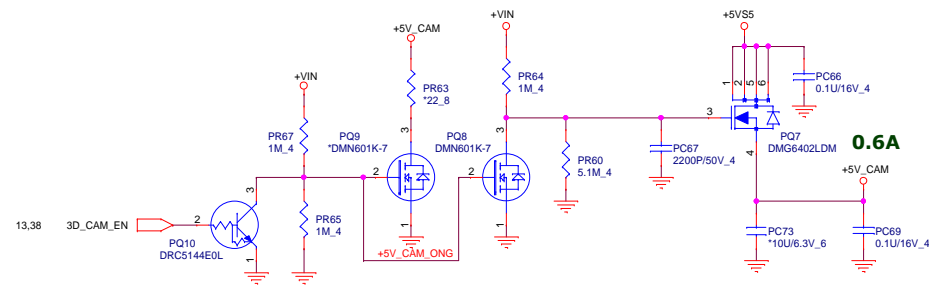


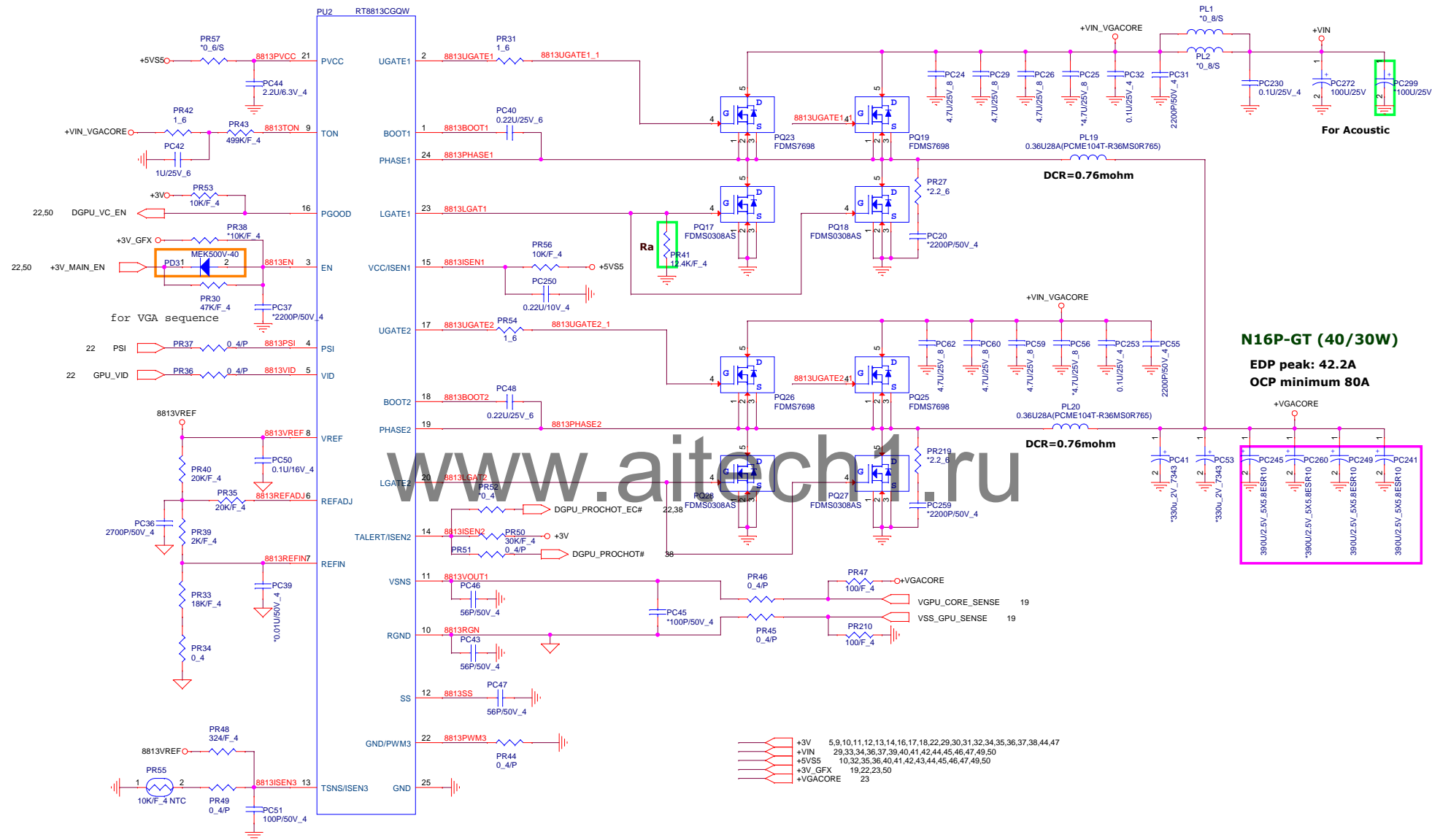


+3V	5,9,10,11,12,13,14,16,17,18,22,29,30,31,32,34,35,36,37,38,44,48
+5V	29,30,31,32,34,35,36,37
+3VS5	10,12,14,16,35,37,38,40,43,50
+5VS5	10,32,35,36,40,41,42,43,44,45,46,48,49,50
+3VSUS	34,36
+3VLAVCC	32,35
+5V_CAM	31
+VIN	29,33,34,36,37,39,40,41,42,44,45,46,48,49,50



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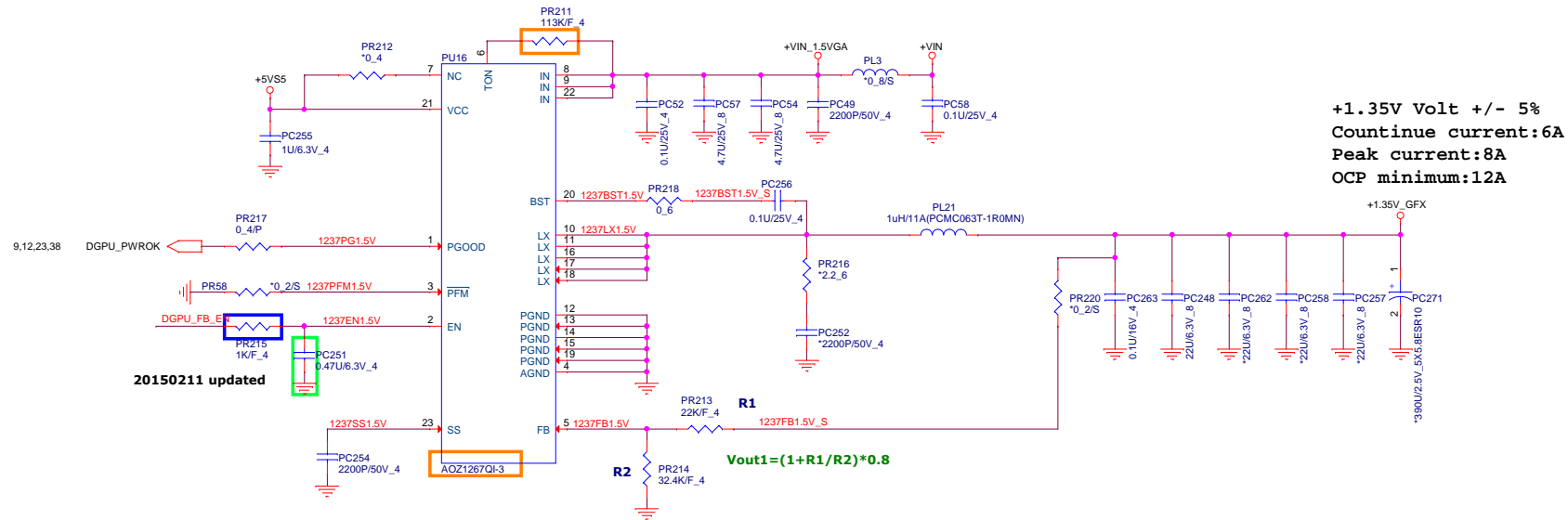




**N16P-GT (40/30W)**  
**EDP peak: 42.2A**  
**OCP minimum 80A**

- +3V 5,9,10,11,12,13,14,16,17,18,22,29,30,31,32,34,35,36,37,38,44,47
- +VIN 29,33,34,36,37,39,40,41,42,44,45,46,47,49,50
- +5VSS 10,32,35,36,40,41,42,43,44,45,46,47,49,50
- +3V\_GFX 19,22,23,50
- +VGACORE 23

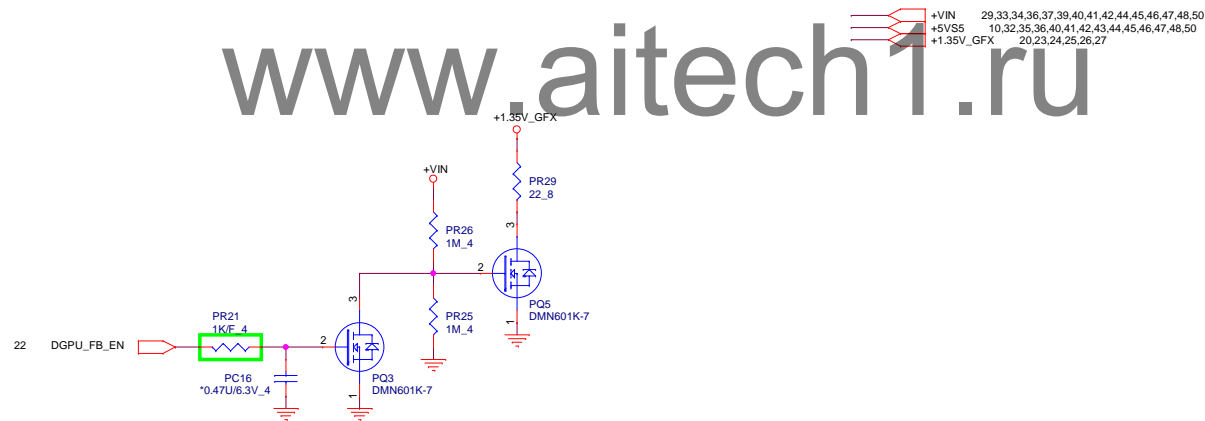
**2015/5/6 updated**



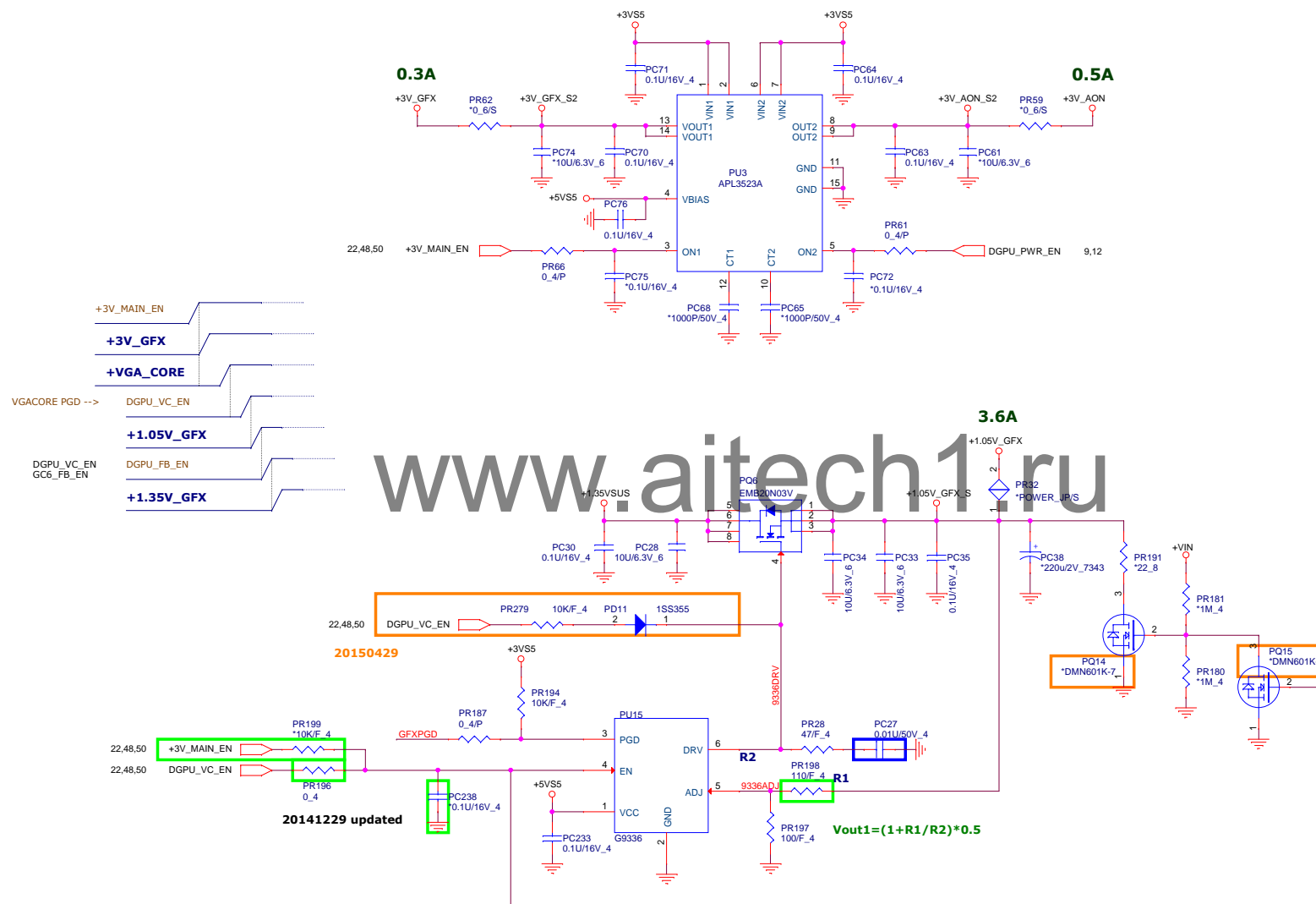
+1.35V Volt +/- 5%  
Continue current:6A  
Peak current:8A  
OCP minimum:12A

$$V_{out1} = (1 + R1/R2) * 0.8$$

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+VIN	29,33,34,36,37,39,40,41,42,44,45,46,47,48,49
+3VS5	10,12,14,16,35,37,38,40,43,47
+5VS5	10,32,35,36,40,41,42,43,44,45,46,47,48,49
+3V_GFX	19,22,23,48
+3V_AON	19,22,23,35
+1.35VSUS	2,6,10,17,18,41,43
+1.05V_GFX	19,20,21,23





**PROJECT :Y11X-6L**  
**Quanta Computer Inc.**

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